NATIONAL SEMICONDUCTOR SYSTEMS & APPLICATIONS GROUP

USER INFORMATION

NS32332 CPU REVISION C

January 21, 1987

This is the new user information sheet for the NS32332 Rev C.

ITEM 1
TITLE /STS Glitch

DESCRIPTION
/STS output may glitch in a slave instruction.

SUGGESTED WORKAROUND AND COMMENTS
Since the glitch occurs in PHI1, it is possible to bypass it by latching the /STS and changing the latch output in PHI2 if no /STS is present (Note that the minimum de-assertion time for /STS from the rising edge of PHI2 is 6 nsec). /STS should be regarded as an early indication of a memory cycle only if a /PAV (/ADS if no MMU) follows it.

AFFECTED REVISIONS: C

ITEM 2
TITLE Wrong BE0-3

DESCRIPTION
The BE0-3 lines may have the wrong value in the operand read cycle (the read from the dispatch table) after a Bus Error or Abort due to an operand fetch.

SUGGESTED WORKAROUND AND COMMENTS
None.

AFFECTED REVISIONS: B2, C

ITEM 3
TITLE Fatal Bus Error

DESCRIPTION
If CPU receives a slave trap under the following conditions, it will stop its execution and assert /MC low with an Idle Status (the same as fatal bus error condition).

- The CPU is executing an FPU instruction which can generate a slave trap with the destination operand being an FPU register.
- an abort on an instruction fetch ahead is pending.
- The instruction immediately following the FPU instruction to be executed has its opcode in the queue and has a memory addressing mode with displacement and the abort on fetch ahead is on fetching the displacement.
- The Bus Interface Unit pipeline is clear.

SUGGESTED WORKAROUND AND COMMENTS

Although the combination of the events is very rare, the bug can be bypassed by removing one of the above conditions. For example FPU instructions which can generate trap can use memory as destination or a NOP can be inserted after an FPU instruction that uses FPU registers as its destination operand.

AFFECTED REVISIONS: C

ITEM 4
TITLE Retried cycle has wrong BE0-3

DESCRIPTION
If a nibble in a Burst operand read cycle is retried (RETRY), the retried bus cycle may have wrong BE0-3.

SUGGESTED WORKAROUND AND COMMENTS
If the BE0-3 have wrong values, the value will be that of the first cycle of the burst. Retry should not be asserted to the CPU if soft errors are detected when burst is in progress.

AFFECTED REVISIONS: C

ITEM 5
TITLE LMR MCR

DESCRIPTION
The instruction "LMR MCR, src" does not flush the internal write validation cache in the CPU. The write validation cache is a three entry cache that keeps the addresses of the last three pages written into by the CPU. Therefore, the MMU can go from no translation to translation without invalidating the entries in the CPU write validation cache and potentially lead to non re-executability on abort.

SUGGESTED WORKAROUND AND COMMENTS
Switching from user to supervisor or vice versa causes flushings of the write validation cache, so the potential for non re-executability upon abort depends on the system software and what it does after turning on the translation. If there is a chance for non re-executability upon abort, then executing a dummy MOVSU instruction before this instruction will cause flushings of the cache. If the instruction sequence may be broken by an interrupt or trace trap, a dummy MOVSU should be inserted before RETT or RETI instructions.

AFFECTED REVISIONS: A4, B, B2, C

ITEM 6
TITLE CPU/ FPU may lose synchronization

DESCRIPTION
During the execution of certain slave instructions that have a memory destination, the CPU after transferring all the operands to the FPU may get aborted due to Abort or Bus Error on one of the following bus cycles:

- A read for effective address calculation of the destination.
- A fetch ahead for a displacement needed to calculate the effective address of the destination.

Since the slave has received all of its operands, it continues execution and it either completes the instruction and asserts a DONE pulse which will be ignored by the CPU, or the slave resets itself when it sees a broadcast slave ID upon execution of any slave instruction in the Abort handler.
The problem is that if the DONE pulse (/SPC or /SDONE) arrives between the /PFS and the broadcast slave ID cycle of the first Slave instruction in the Abort handler, the synchronization between the CPU and the slave will be lost. The following is the list of the instructions that are susceptible to this bug:

Format 9, 15.1 - MOVLF, MOVFL, ROUND, TRUNC, FLOOR, SFSR and counterpart Custom Slave instructions
Format 11, 15.5 - MOVf, NEGf, ABSf and counterpart Custom Slave instructions
Format 12, 15.7 - SQRTf, LOGBf, COSIf and counterpart Custom Slave instructions

SUGGESTED WORKAROUND AND COMMENTS
The probability of the occurance of this failure is very low due to the combination of the events that must be true and the narrow time window. To bypass this bug the DONE pulse from the Slave should not appear in the narrow window mentioned above. To avoid this, the execution of the first slave instruction in the Abort/Bus Error handler should be delayed until the aforementioned instructions complete their execution and return the DONE pulse.
It takes the 32332 a minimum of 45 clock cycles from receiving an Abort/Bus Error to execution of the first instruction of the exception handler. If the slave sends the DONE pulse within 45 clock cycles after receiving the last operand, then there is no problem.
The only instructions in the above list that have longer execution times than 45 clock cycles are ROUND, TRUNC, FLOOR, SQRTf and COSIf (note that the Custom Slave instruction execution times depend on their implementation). The worst case execution time for ROUND, TRUNC, and FLOOR minus the 45 clock cycles yields 15 clock cycles. Thus, the first slave instruction in the exception handler should be executed no earlier than 15 cycles from the first non-sequential instruction fetch in that exception handler. As for SQRTf and COSIf, they have not been implemented by National FPU devices.

AFFECTED REVISIONS: A4, B, B2, C

ITEM 7
TITLE /MC bug

DESCRIPTION
If /MC signal is low while STO-3 have a value of zero, a fatal bus error is indicated. In the following cases for a period of one clock cycle or less /MC is low while STO-3 indicate idle

status (zero).
1- /MC is activated while the BIU is performing a non-sequential fetch during an abort acknowledge sequence. If the non-sequential fetch bursts, status lines may change their values from 9 to 0 during PHI1 T4 of the last nibble. /MC will return high a cycle later during PHI1 Ti.
2- /MC is activated during an operand transfer that crosses a page boundary. If this operand transfer bus cycle gets terminated by an abort or bus error, the /MC and the status signals will change at the same time. Thus /MC*(ST0-3=0) may glitch.

SUGGESTED WORKAROUND AND COMMENTS
A fatal bus error should be detected if /MC*(ST0-3=0) is active for two clock cycles.

AFFECTED REVISIONS: B, B2, C

The interior of the NS32332 package contains a small amount of Beryllium Oxide, a substance that may pose a health hazard when inhaled. Normal use and application should pose no health hazard to the end user.

WARNING: USE CAUTION IN DISPOSAL. DO NOT COMPACT OR GRIND UP SO THAT INHALATION OF THE COMPACTED REMAINS OF THE PART IS POSSIBLE.

If it is necessary to dispose of the microprocessor, avoid inhalation of the compacted remains of the part. National Semiconductor Corporation recommends that the NS32332 microprocessor be returned to NSC for disposal.

USER INFORMATION

NS32c201 TCU Revision B

December 4, 1986

1. Under heavy current loads, the switching transients may cause the low level voltages on the output signals to reach levels higher than those specified in the data sheet. This problem can be avoided by reducing the load on the output signals and using 'ROGERS' type capacitors as bypassing caps. Note that the part is specified to sink 2 mA when Vol is at 0.10Vcc (MAX for Vol). This is not the same as the NS32201 which is specified to sink 20 mA when Vol is at 0.5 volts.

USER INFORMATION

NS32382 MMU

August 25, 1986

ITEM #1
TITLE None

DESCRIPTION
There are no known bugs in this part.

USER INFORMATION

NS32081 FPU, Revision H

August 11, 1986

DOCUMENTATION CLARIFICATION

The following are clarifications or corrections to the current NS32081 FPU documentation:

1. When the FPU signals that it is finished processing an instruction (by pulsing the SPC pin low), it is necessary to wait for at least two cycles of the clock (CLK) before reading the Status Word. Series 32000 CPU's satisfy this requirement.

2. After reading the Status Word from the FPU, it is necessary to wait for three cycles of the CLK clock before reading a result. Series 32000 CPU's satisfy this requirement.

3. Whenever an FPU error condition occurs, the FSR TT field is loaded with the error code, regardless of whether that condition is enabled to cause a trap. An FPU instruction can therefore complete normally and still display a code of 001 (Underflow) or 110 (Inexact Result). This code remains in the TT field only until the next floating-point instruction (other than SFSR) completes. Early documentation has strongly implied that the TT field will appear non-zero only if a trap actually occurs. This has been fixed in the Series 32000 Instruction Set Reference Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

4. The FSR TT field is loaded with a new error status value (zero if no error) at the end of every floating-point instruction except LFSR or SFSR. (The LFSR instruction loads the TT field, but with the value supplied by the programmer instead of with error status). Most documentation to date, however, has stated that the FSR TT field is altered only if an error occurs or if the LFSR instruction is executed. The necessary changes appear in the Series 32000 Instruction Set Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

5. Asynchronous timing of SPC pulses with respect to CLK does not work reliably. Transfers to the FPU must follow NS32000-series CPU timing exactly: i.e., the SPC pulse must start shortly after a CLK rising edge and terminate shortly after the next rising edge. If the FPU is used as a Slave Processor with a Series 32000 CPU, it should be clocked with the TCU CTTL signal. The necessary changes have been made in the Series 32000 Databook.

6. When transferring the ID Byte and the Operation Word to the FPU, there must be a gap of at least one clock cycle between T4 of the ID Byte transfer and T1 of the Operation Word transfer. Failure to do this can make register-to-register forms of FPU instructions execute unreliably. This requirement is met by 32000-series CPU's. Data sheets and Application Note AN383 do not yet mention it.

7. The minimum clock frequency (CLK pin) is 4 Mhz instead of 200 Khz as stated in the data sheet.

8. When the FPU is used in a system that includes the MMU, the FPU RST pin must be tied to the system reset, not the RST/ABT pin of the MMU.

USER INFORMATION

NS32332 CPU, Revision B

September 29, 1986

This is the new user information sheet for the NS32332.

ITEM #1
TITLE RDVAL, WRVAL

DESCRIPTION
The RDVAL, WRVAL instructions are not functional.

SUGGESTED WORKAROUND AND COMMENTS
These instructions should be simulated by software. For example RDVAL R3 can be replaced by a branch (BSR) to WRDVAL. Here WRDVAL routine simulates RDVAL R3 and returns the result in the flag bit of the PSR register.

```
w_rdval:
   bicpsrw   $0x800        #turn off interrupts
   save      [r6, r7]
   movd      r3, r7
   ashd      $-14, r7      #index into ptel table
   andd      $0x3fC, r7
   addd      _uptel, r7    #the R3 address corresponding
                           #entry in ptel
   tbitb     $2, 0(r7)     #is read ok?
   bfc       w_bad         #no read, return error
   tbitb     $0, 0(r7)     #is the address valid?
   bfc       w_bad         #no, MMU should abort
   movd      r3, r6        #get pte2 entry
   ashd      $-7, r6
   andd      $0x1FFF8, r6
   addd      _upte2, r6    #the R3 address corresponding
                           #entry in pte2
   tbitb     $2, 0(r6)     #is read ok?
   bfc       w_bad
   bicpsrb   $2x20         #rdval is ok
w_ret:
   restore   [r6, r7]
   bispsrw   $0x800        #enable interrupts
   ret       0             #return
w_bad:
   bispsrw   $0x20         #rdval failed, set flag bit
   br        w_ret
```

AFFECTED REVISIONS: A4, B, B2

ITEM #2
TITLE ILO HOLD

DESCRIPTION
If the /HOLD input is asserted while CBITIi or SBITIi is being

executed, the NS32332 CPU will assert the /HLDA output and continues to stay in this state even when /HOLD is deasserted.

SUGGESTED WORKAROUND AND COMMENTS
The /HOLD should be synchronized to the /ADS output.

AFFECTED REVISIONS: A4, B, B2

ITEM #3
TITLE INT STRING

DESCRIPTION
If /NMI or /INT get asserted during the execution of one of the instructions, MOVSi, MOVST, SKPSi, SKPST, CMPSi, CMPST, WAIT, the first Interrupt Acknowledge status may be 0101 instead of 0100. Also in the case of /INT, the first End of Interrupt status may be 0111 instead of 0110.

SUGGESTED WORKAROUND AND COMMENTS
This bug should not create any problem unless the status bits are 'being decoded to differentiate master and cascaded interrupt acknowledge/ return from interrupt cycles.

AFFECTED REVISIONS: A4, B, B2

ITEM #4
TITLE PRE-FETCH ABORT WITH INTERRUPTS

DESCRIPTION
If a pre-fetch cycle gets aborted and an external interrupt (/INT, /NMI) is asserted within a certian time from the ABORT, the NS32332 may halt execution and float its outputs pins. This bug is very rare due to the exact timings it requires.

SUGGESTED WORKAROUND AND COMMENTS
/INT or /NMI should be synchronized to the /PFS output.

AFFECTED REVISIONS: A4, B

ITEM #5
TITLE NMI

DESCRIPTION
/NMI input may be ignored by the NS32332 if it is asserted at a certain time with respect to the internal state of the NS32332.
SUGGESTED WORKAROUND AND COMMENTS
None

AFFECTED REVISIONS: A4, B

ITEM #6
TITLE BURST WITH FLOAT

DESCRIPTION
/BOUT (formerly /BREQ) gets asserted regardless of the state of the /FLT input. Note that /BOUT should get asserted after the

/FLT input is deactivated.

SUGGESTED WORKAROUND AND COMMENTS
None

AFFECTED REVISIONS: A4, B

ITEM #7
TITLE MIXING FAST AND SLOW SLAVE PROTOCOL

DESCRIPTION
If a slave instruction is being executed with the slow slave protocol, the upper byte (AD24:31) is xxxxxxxx instead of xxxxxxxl when the CPU issues the ID byte (status F). A fast slave may understand this as its ID byte and initiate its protocol with the CPU resulting in bus contention.

SUGGESTED WORKAROUND AND COMMENTS
None, however the probability of failure due to this bug is low.

AFFECTED REVISIONS: A4, B, B2

ITEM #8
TITLE LMR MCR

DESCRIPTION
The instruction "LMR MCR, src" does not flush the internal write validation cache in the CPU. Therefore, the MMU can go from no translation to translation without invalidating the entries in the CPU write validation cache and lead to non re-executability on abort.

SUGGESTED WORKAROUND AND COMMENTS
Executing a dummy MOVSU instruction before this instruction will cause flushings of the write validation cache. If the instruction sequence may be broken by an interrupt or trace trap, a dummy MOVSU should be inserted before RETT or RETI instructions.

AFFECTED REVISIONS: A4, B, B2, C

The interior of the NS32332 package contains a small amount of Beryllium Oxide, a substance that may pose a health hazard when inhaled. Normal use and application should pose no health hazard to the end user.

WARNING: USE CAUTION IN DISPOSAL. DO NOT COMPACT OR GRIND UP SO THAT INHALATION OF THE COMPACTED REMAINS OF THE PART IS POSSIBLE.

If it is necessary to dispose of the microprocessor, avoid inhalation of the compacted remains of the part. National Semiconductor Corporation recommends that the NS32332 microprocessor be returned to NSC for disposal.

NS32332

PRODUCT UPDATE

NS32332 CPU Revision D

PRODUCT DATA SHEET CHANGE/CLARIFICATION:

1. The /MC should be detected as valid if it holds its value for two consecutive clock cycles.
2. If the NS32332 is executing an instruction which results in a jump and thus a queue flush, and its BIU is prefetching via bursting, the burst will be terminated before the address reaches an appropriate boundary (i.e. 16 byte boundary in the 32 bit bus mode). In this case /BOUT will be deasserted indicating an internal termination of the burst.
3. In the NS32332 data sheet, there is no MAX specified for tBERh. The state after detecting a Bus Error in T4 state is a Ti. The Bus Error should be deasserted to the CPU at the latest in the beginning of the cycle following this Ti cycle.
4. The opcodes for the LCR and SCR instructions are incorrect as shown in the data sheet. The correct opcodes are 0010 and 0011 for LCR and SCR, respectively.
5. The Max for AC parameter tDr has been changed to 38 and 50 ns at 15 and 10 Mhz respectively. This parameter is measured relative to the PHI1 RE of the state T3.
6. As of revision D, the NS32c201 should be used to provide the PHi clocks of the NS32332. This is due to the tightening of the non-overlap timing specification (tnOVL) for the NS32332. The NS32c201 provides the required PHi signals for the NS32332.
7. Output leakage current, Io(OFF), for AD pins (AD pins in TRI-STATE condition) is as follows: -150 microamps when Vout = 0.4 volts +1 mA when Vout = Vcc +350 microamps when Vout = 2.4 volts For the remaining output pins the output leakage current is -60 and +60 microamps when Vout is at 0.4 volts and Vcc respectively.
8. The maximum for the active supply current (Icc max) is 600 mA.
9. The minimum Vch is 4.25 volts when the part is operating in the 4.5-4.75 voltage range (10% tolerance part).

NS32c201

PRODUCT UPDATE

NS32c201 TCU Revision C

PRODUCT INFORMATION:

1. Description: Under heavy current loads, the switching transients may cause the low level voltages on the output signals to reach levels higher than those specified in the data sheet.

   Workaround: This problem can be avoided by reducing the load on the output signals and using 'ROGERS' type capacitors as bypassing caps. Note that the part is specified to sink 2 mA when Vol is at 0.10Vcc (MAX for Vol). This is not the same as the NS32201 which is specified to sink 20 mA when Vol is at 0.5 volts.

2. Description: The output signals of this revision of the NS32c201 may exhibit overshoot/ undershoot when switching from one state to another. The magnitude of the spikes depend on several conditions such as loading of the TCU outputs, placing of the TCU relative to the rest of the cluster, robustness of the TCU Vcc and GND inputs decoupling and the inductance of the TCU socket and the PC board traces.

   Workaround: Therefore, it is recommended that zero ohm resistors be inserted on the PHIi paths to provide the capabality for slowing these signals in case the overshoot/ undershoot make the PHIi levels out of the CPU spec. It is further recommended that the TCU be soldered into the board to minimize inductance of the paths from the PCB Vcc and GND planes the to TCU Vcc and GND pins.

3. Description: During reset (/RSTI input held low), the TCU will stop clocking if the /RWEN/SYNC input is high.

4. Description: The minimum Voh for PHI1 and PHI2 is 4.25 volts when the parts is operating at 4.5 volts (10% tolerance part).

NATIONAL SEMICONDUCTOR
SYSTEMS & APPLICATIONS GROUP
APPLICATIONS BULLETIN 4

USE of the NS32332 with the NS32082 and the NS32201

February 4, 1986

Care should be taken when the NS32332 is designed in a system with the NS32201 and the NS32082. Two configurations need to be considered, one with MMU and one without.

In a configuration without an MMU, TCU and CPU both run a four clock cycle bus (figure 1). The RDY signal is the only incompatible signal between the CPU and the TCU and therefore the RDY output of the TCU should not be directly connected to the RDY input of the NS32332. The NS32332 samples its RDY input in the middle of T3 while the NS32201 asserts its RDY output shortly after the middle of T2 and removes it shortly after the middle of T3, thus the NS32332 RDY input hold time (tRDYh) is not met. To meet tRDYh, the RDY output of the NS32201 should be clocked by the rising edge of the CTTL using a D type flip-flop (74AS74) and then taken to the NS32332. It should be noted that the NS32332 outputs the data in a write cycle in T3 unless DT/SDONE pin is sampled low on the rising edge of the reset in which case the data is output during T2. The DT/SDONE pin is implemented as of revision B of the NS32332.

In a configuration with MMU the NS32332 runs a four clock cycle bus while the NS32082 runs a five cycle bus. Two options can be exersized.

The first optiqn is extending the NS32332 bus cycle to five clocks by adding a blind wait state that bypasses the NS32201 (figure 2). This configuration generally requires the minimum hardware modification for a 320xx based design to run the NS32332. Here the NS32201 output signals can be used to interface the NS32332 and the NS32082 to the memory or I/O. Additional wait states can be inserted by clocking the RDY output of the TCU.

The second option is to have the NS32332 run a four clock cycle bus (figure 3). In this configuration the NS32201 output signals can not be used to interface the NS32332 to memory or I/O; they can only be used to interface the NS32082 to the memory. In this configuration a revision N of the NS32082 should be used.

332, TCU timing diagram, NO wait state, No MMU

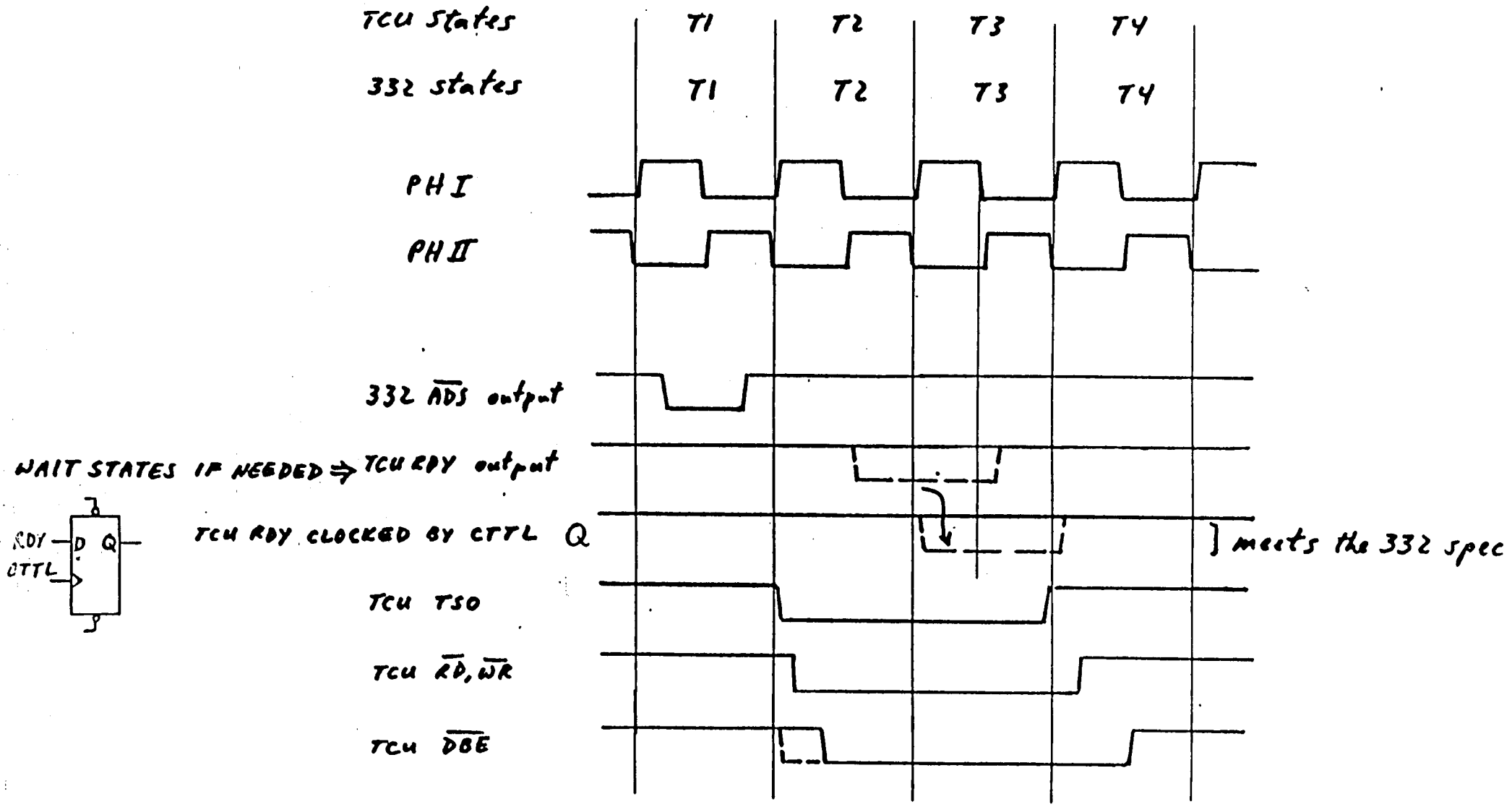

Figure 1

similar to timing diagram of 332 adapter to DB32000

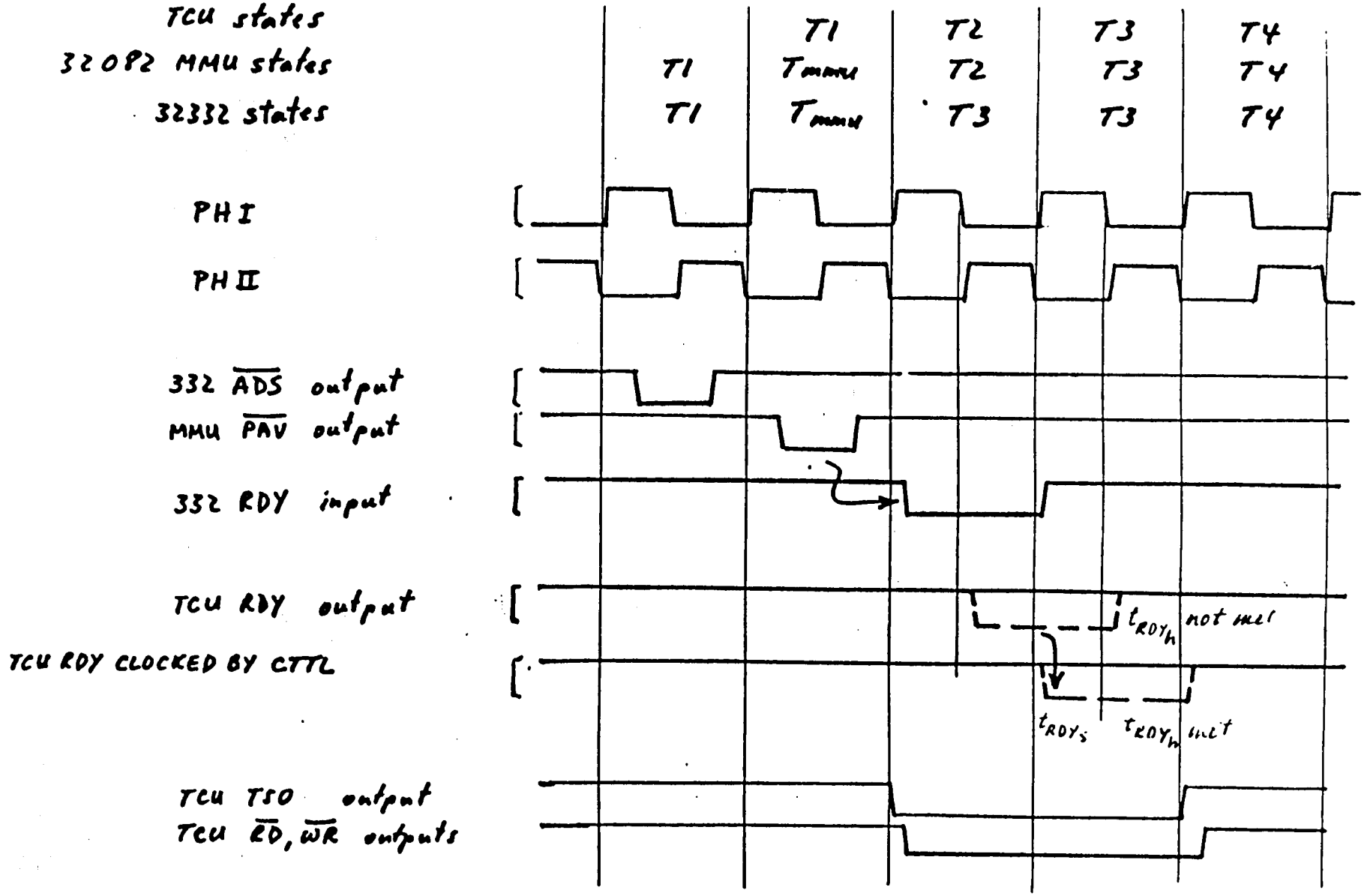

Figure 2

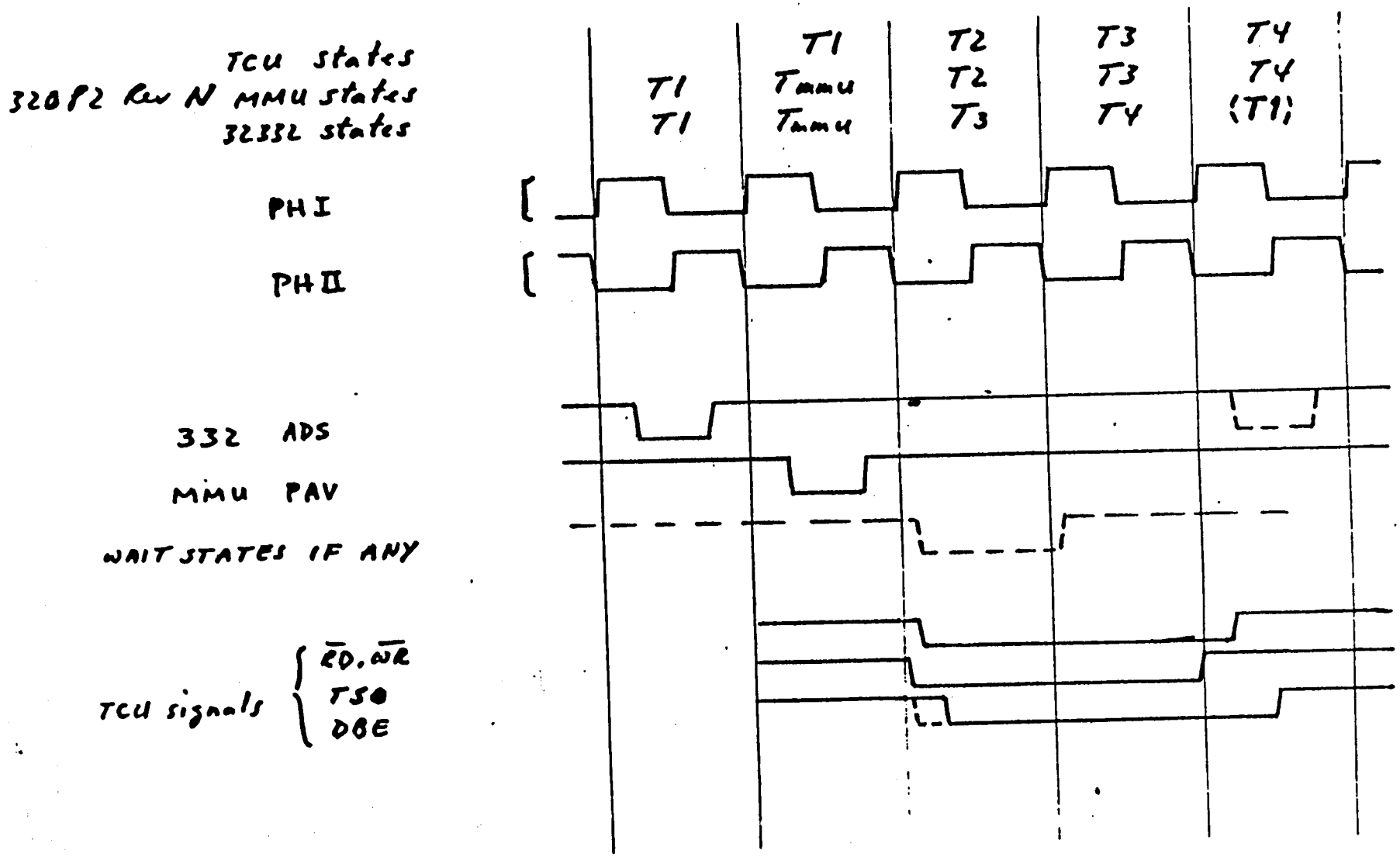
TCU states
32082 Rev N MMU states
32332 states
T1
T1
T1
Tmmu
Tmmu
T2
T2
T3
T3
T4
T4
(T1)
PH I
PH II
332 ADS
MMU PAV
WAIT STATES IF ANY
TCU signals
RD, WR
TSO
DBE

Figure 3