This document contains a collection of technical status information sheets about the Series 32000 products provided by National Semiconductor. These sheets, like standard data sheets, were available to the public. They were published in February 1989.

It is interesting to read which kind of problems the designers were detecting in their products. This makes visible the complexity of a chip.

February 2014

32K Tech Notes List 1 FEB 89

USER INFORMATION

NS32008-6 CPU, Revision C

June 23, 1986

1. The instructions CMPF and CMPL, if they generate a Trap(FPU), may cause the CPU to read the trap's interrupt descriptor from an address other than INTBASE + h'0C, or they may bring the CPU to an internal deadlock, requiring a reset. The bad address will be in the range INTBASE + h'2000 through INTBASE + h'327FC, depending on the exact encoding of the most significant 16 bits of the Basic Instruction field of the instruction. Note that the only condition under which these instructions will generate Trap(FPU) is when they are given a Reserved operand value. See the Instruction Set Manual, Section 3.3.

2. The Floating-Point instructions:

```
FLOORLB, FLOORLW
ROUNDLB, ROUNDLW
TRUNCLB, TRUNCLW
```

   will fail if the source operand is an immediate value, by bringing the CPU and FPU to a mutual deadlock. The CPU causes this deadlock by not issuing the whole immediate operand to the FPU.

3. Shift instructions of the form:

```
LSHW    any-source,TOS
LSHD    any-source,TOS
ASHW    any-source,TOS
ASHD    any-source,TOS
```

   may misinterpret the sign and magnitude of the first operand, causing an incorrect shift direction and count. Use 0(SP) instead of TOS to bypass this problem.

4. In executing the RETT instruction, the CPU will sometimes read the MOD register value from the wrong address, and also with incorrect byte order and/or missing bytes. The related instruction RETI does not fail in this manner in an NS32008. The incorrect address will be offset by a small amount (+/- 1 byte) from the correct address. The instruction continues by attempting to read the SB value from the incorrect address in the MOD register. This problem is associated with a specific set of timing sequences on the bus,

involving HOLD/HLDA DMA and/or WAIT states.

5. DMA requests made to the CPU on the HOLD pin may cause the CPU to lock up if they are made during the T1, T3 or Ti CPU states. HOLD requests should be synchronized to the rising edge of PHI1, should be asserted only during T2 or T4 and should be inhibited during slave operations. This problem is very unlikely to occur.

6. The M bit of the CFG register is stuck to a 1. This prevents MMU instructions from generating a Trap (UND).

7. The DEIi instruction may generate invalid results when the quotient part overflows by more than one bit. In this case the quotient should be truncated and the remainder should have the correct value.

8. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states. 9. Address lines A8-A15 are not hold stable through the entire bus cycle. An address latch is necessary, triggered by the Address Strobe (ADS), in addition to the one needed for A0-A7.

DATA SHEET CLARIFICATION
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1. A 10K pull-up resistor is required on the SPC/AT line.

2. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

3. The minimum clock frequency for the 32000 family processors, CPU, MMU, and FPU, is 4 Mhz instead of 200 Khz as stated in the data sheets.

USER INFORMATION

NS32008 CPU, Revision D

June 23, 1986

1. The DEIi instruction may generate invalid results when the quotient part overflows by more than one bit. In this case the quotient should be truncated and the remainder should have the correct value.

2. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

3. Address lines A8-A15 are not hold stable through the entire bus cycle. An address latch is necessary, triggered by the Address Strobe (ADS), in addition to the one needed for A0-A7.

DATA SHEET CLARIFICATION
---

1. A 10K pull-up resistor is required on the SPC line.

2. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

3. The minimum clock frequency for the NS32008 is 4 MHz instead of 200 Khz as stated in the data sheet. At this frequency the maximum clock high voltage (on the PHI1, PHI2 Pins) is Vcc instead of Vcc + 0.5 Volt.

USER INFORMATION

NS32008 CPU, Revision E

May 29, 1987

1. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

2. This revision of the NS32008 can not tolerate overlap (negative non-overlap) on the clock inputs. Therefore, it is strongly recommended that this revision of the NS32008 be used with the NS32201. The NS32c201 should not be used with this revision of the NS32008 since its clock outputs may overlap as much as 1 nsecond.

3. The format 14 instructions with opcode 00xx do not trap undefined as they should. The above instructions should not be used with this revision of the NS32008.

DATA SHEET CLARIFICATION
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1. A 10K pull-up resistor is required on the SPC line.

2. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

3. The minimum clock frequency for the NS32008 is 4 MHz instead of 200 Khz as stated in the data sheet. At this frequency the maximum clock high voltage (on the PHI1, PHI2 Pins) is Vcc instead of Vcc + 0.5 Volt.

4. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

USER INFORMATION

NS32016 CPU, Revision M

June 19,1985

1. The instructions CMPF and CMPL, if they generate a Trap(FPU), may cause the CPU to read the trap's interrupt descriptor from an address other than INTBASE + h'0C, or they may bring the CPU to an internal deadlock, requiring a reset. The bad address will be in the range INTBASE + h'2000 through INTBASE + h'327FC, depending on the exact encoding of the most significant 16 bits of the Basic Instruction field of the instruction. Note that the only condition under which these instructions will generate Trap(FPU) is when they are given a Reserved operand value. See the Instruction Set Manual, Section 3.3.

   MMU instructions can also trigger the above symptoms if a Rev. K1 or earlier MMU is used and DMA requests are occurring using the HOLD pin. However, this is only one side effect of an MMU malfunction that is often fatal in other ways.

2. The Floating-Point instructions:

```
FLOORLB, FLOORLW
ROUNDLB, ROUNDLW
TRUNCLB, TRUNCLW
```

   will fail if the source operand is an immediate value, by bringing the CPU and FPU to a mutual deadlock. The CPU causes this deadlock by not issuing the whole immediate operand to the FPU.

3. Shift instructions of the form:

```
LSHW    any-source,TOS
LSHD    any-source,TOS
ASHW    any-source,TOS
ASHD    any-source,TOS
```

   may misinterpret the sign and magnitude of the first operand, causing an incorrect shift direction and count. Use 0(SP) instead of TOS to bypass this problem.

4. In executing the RETT instruction, the CPU will sometimes read the MOD register value from the wrong address, and also with incorrect byte order and/or missing bytes. The related

instruction RETI does not fail in this manner in an NS32016. The incorrect address will be offset by a small amount (+/- 1 byte) from the correct address. The instruction continues by attempting to read the SB value from the incorrect address in the MOD register. This problem is associated with a specific set of timing sequences on the bus, involving HOLD/HLDA DMA and/or WAIT states. It can be bypassed (in an NS32016 only) by aligning the RETT instruction so that it occupies one word (16 bits) on an even address, and is therefore fetched in one memory cycle. Doing this prevents the sequences that lead to this failure.

5. DMA requests made to the CPU on the HOLD pin may cause the CPU to lock up if they are made during the T1, T3 or Ti CPU states. HOLD requests should be synchronized to the rising edge of PHI1, should be asserted only during T2 or T4 and should be inhibited during slave operations. This problem is very unlikely to occur.

6. The DEIi instruction may generate invalid results when the quotient part overflows by more than one bit. In this case the quotient should be truncated and the remainder should have the correct value.

7. There is a potential for a problem at 10 Mhz when the CPU addresses the 128 bytes residing in the virtual address range FFFF80 to FFFFFF. The problem manifests itself in changing of the address bit 22 (A22) from a '1' to a '0' while ADS is still low. This problem can be worked around by not addressing the FFFF80..FFFFFF address range.

8. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

9. A very small number of CPUs with date code prior to 8532 may malfunction at high temperature and 10 MHz when 'register' addressing mode is specified. If the problem occurs the CPU selects a wrong operand address. The problem does not occur on devices with a more recent date code or shipped directly by National after 11-1-85.

10. The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer lenght than the one specified by the instruction. This problem occurs only if scaled indexing mode is used with TOS or REG addressing mode for gen1 operand. This problem will cause the instructions

EXTSi and FFSi to generate wrong results. For other instructions however, this problem is not harmful unless the read crosses a page boundary and results in a page fault.

DATA SHEET CLARIFICATION
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1. A 10K pull-up resistor is required on the SPC/AT line.

2. As of Revision N of the CPU, it is no longer true that the CPU floats its ADS pin when the FLT signal is received from the MMU. The ADS pin no longer needs to be connected to a pull-up resistor unless a DMA controller is being used in the system.

3. The HBE signal is normally floated when the CPU grants the bus in response to a DMA request on the HOLD pin. However, when an MMU is used and the bus is granted during an MMU page table look up, HBE is not floated since the CPU does not have sufficient information to synchronize the release of HBE to the MMU's bus cycles. Therefore, in a memory managed system, an external tri-state buffer is required.

4. In systems containing an MMU, the HBE signal should not be latched externally on the rising edge of the PAV pulse as addresses are. When the MMU performs a Page Table access, and then removes the FLT signal to the CPU, there is a delay from the point that FLT is inactive to the point that HBE is valid which causes such latching to be unreliable at higher clock rates. See Figure 4-9 in the NS32016 data sheets, timing parameter tHBEr.

5. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

6. The minimum clock frequency for the NS32016 is 4 MHz instead of 200 kHz as stated in the data sheet. At this frequency the maximum clock high voltage (on PHI1, PHI2) pins is Vcc instead of Vcc + 0.5 Volt.

USER INFORMATION

NS32016 CPU, Revision N

March 26, 1987

1. During the instructions MULi, MEIi, DEIi and LPRi, if an Abort trap occurs on the second operand, this may cause the wrong Interrupt Table entry to be referenced, and thereby cause the Abort to transfer control to the wrong interrupt/trap service routine. The service routine actually invoked will depend on the value of the first operand (MUL, MEI, DEI), or on the state in which a previous instruction leaves the CPU (LPR) and is therefore unpredictable in general. However, it appears that the specific cases "LPR PSR" and "LPR INTBASE" will consistently transfer control to the Trap(ILL) service routine when this failure occurs. This problem is often associated with either HOLD/HLDA DMA or WAIT states.

2. The Floating-Point instructions:

   FLOORLB, FLOORLW
   ROUNDLB, ROUNDLW
   TRUNCLB, TRUNCLW

   will fail if the source operand is an immediate value, by bringing the CPU and FPU to a mutual deadlock. The CPU causes this deadlock by not issuing the whole immediate operand to the FPU.

3. The instructions CMPF and CMPL, if they generate a Trap(FPU), may cause the CPU to read the trap's interrupt descriptor from an address other than INTBASE + h'0C, or they may bring the CPU to an internal deadlock, requiring a reset. The bad address will be in the range INTBASE + h'2000 through INTBASE + h'327FC, depending on the exact encoding of the most significant 16 bits of the Basic Instruction field of the instruction. Note that the only condition under which these instructions will generate Trap(FPU) is when they are given a Reserved operand value. See the Instruction Set Manual, Section 3.3.

   MMU instructions can also trigger the above symptoms if a Rev. K1 or earlier MMU is used and DMA requests are occurring using the HOLD pin. However, this is only one side effect of an MMU malfunction that is often fatal in other ways.

4. If an interrupt is set pending near the end of an instruction that branches, and the target of the branch is in an invalid page, an abort can occur after the interrupt has begun internal service within the CPU. Two results of this have been reported:

   1) When the Abort trap is taken the I, P and S bits of the

PSR image on the stack may be cleared. In most systems this damage can be repaired by the Abort trap service routine, using the rule that if the U bit of the PSR image is set, then the S and I bits should also be set.

2) When the Abort trap is taken, the PSR, MOD and PC images may be stored to the wrong addresses near the top of the Interrupt Stack. This is fatal if it is allowed to occur.

Both manifestations of this bug may be bypassed by synchronizing the INT and NMI inputs so that they become active during the PFS pulse from the CPU. The NMI pulse from the MMU must bypass this synchronization in order to perform Interrupt-Mode breakpointing correctly. MMU Execution breakpoints must never be used in Interrupt Mode, as they can trigger this bug.

5. The following instruction forms should not appear after an instruction with an operand of access class "rmw":

```
ADDR    Rj[Rx:i],anydest
CHECKi  anyreg,Rj[Rx:i],anysource
CVTP    anyreg,Rj[Rx:i],anydest
```

Doing so can cause the effective address of the first general operand to be computed incorrectly. Use instead the form 0(Rj)[Rx:i], which is identical in effect to Rj[Rx:i] but is not susceptible to this bug.

6. Shift instructions of the form:

```
LSHW    any-source,TOS
LSHD    any-source,TOS
ASHW    any-source,TOS
ASHD    any-source,TOS
```

may misinterpret the sign and magnitude of the first operand, causing an incorrect shift direction and count. Use 0(SP) instead of TOS to bypass this problem.

7. In executing the RETT instruction, the CPU will sometimes read the MOD register value from the wrong address, and also with incorrect byte order and/or missing bytes. The related instruction RETI does not fail in this manner in an NS32016. The incorrect address will be offset by a small amount (+/- 1 byte) from the correct address. The instruction continues by attempting to read the SB value from the incorrect address in the MOD register. This problem is associated with a specific set of timing sequences on the bus, involving HOLD/HLDA DMA and/or WAIT states. It can be bypassed (in an NS32016 only) by aligning the RETT instruction so that it occupies one word (16 bits) on an even address, and is therefore fetched in one memory cycle. Doing this prevents the sequences that lead to this failure.

8. DMA requests made to the CPU on the HOLD pin may cause the CPU to lock up if they are made during the T1, T3 or Ti CPU states. HOLD requests should be synchronized to the falling edge of PHI1,should be asserted only during T2 or T4 and should be inhibited during slave operations. This problem is very unlikely to occur.

9. At higher ambient temperatures (above 40 degrees C), the CPU may perform interrupt service more than once in response to a pulse on the NMI pin.

10. The DEIi instruction may generate invalid results when the quotient part overflows by more than one bit. In this case the quotient should be truncated and the remainder should have the correct value.

11. There is a potential for a problem at 10 Mhz when the CPU addresses the 128 bytes residing in the virtual address range FFFF80 to FFFFFF. The problem manifests itself in changing of the address bit 22 (A22) from a '1' to a '0' while ADS is still low. This problem can be worked around by not addressing the aforementioned address range.

12. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

13. A very small number of CPUs with date code prior to 8532 may malfunction at high temperature and 10 MHz when 'register' addressing mode is specified. If the problem occurs the CPU selects a wrong operand address. The problem does not occur on devices with a more recent date code or shipped directly by National after 11-1-85.

14. If a RDVAL or a WRVAL is being executed and either the effective address to be validated or any data necessary to calculate that address reside in an invalid page, resulting in a page fault, the cpu and the mmu will get out of synchronization. This problem can be easily worked around by ensuring that no page fault occurs while the cpu is obtaining the effective address to be validated.

15. If any of the instructions BICPSRW, BISPSRW, LPRi, LMR is executed in user mode, the PSR pushed on the interrupt stack, as a result of the trap (ILL) execution, may get corrupted. This occurs only when the above instructions are used with the operand in memory and several wait states (at least 26 cycles) are inserted in the last memory read cycle. This however is not a serious problem since the above instructions are not intended to be used by the user mode programs.

16. The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer lenght than the one specified by the instruction. This problem occurs only if scaled indexing mode is used with TOS or REG addressing mode for gen1 operand.

This problem will cause the instructions EXTSi and FFSi to generate wrong results. For other instructions however, this problem is not harmful unless the read crosses a page boundary and results in a page fault.

DATA SHEET CLARIFICATION
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1. As of Revision N of the CPU, it is no longer true that the CPU floats its ADS pin when the FLT signal is received from the MMU. The ADS pin no longer needs to be connected to a pull-up resistor unless a DMA controller is being used in the system.

2. A 10K pull-up resistor is required on the SPC/AT line.

3. The HBE signal is normally floated when the CPU grants the bus in response to a DMA request on the HOLD pin. However, when an MMU is used and the bus is granted during an MMU page table look up, HBE is not floated since the CPU does not have sufficient information to synchronize the release of HBE to the MMU's bus cycles. Therefore, in a memory managed system, an external tri-state buffer is required.

4. In systems containing an MMU, the HBE signal should not be latched externally on the rising edge of the PAV pulse as addresses are. When the MMU performs a Page Table access, and then removes the FLT signal to the CPU, there is a delay from the point that FLT is inactive to the point that HBE is valid which causes such latching to be unreliable at higher clock rates. See Figure 4-9 in the NS32016 data sheets, timing parameter tHBEr.

5. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with the falling edge of CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

6. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

7. The minimum clock frequency for the NS32016 is 4 MHz instead of 200 kHz as stated in the data sheet. At this frequency the maximum clock high voltage (on PHI1, PHI2) pins is Vcc instead of Vcc + 0.5 Volt.

USER INFORMATION

NS32016 CPU, Revision R

March 26, 1987

1. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

2. There is a potential for a problem at 10 Mhz when the CPU addresses the 128 bytes residing in the virtual address range FFFF80 to FFFFFF or 7FFF80 to 7FFFFF. The problem manifests itself in changing of the address bit 22 (A22) from a '1' to a '0' while ADS is still low. This problem is screened for and cpu's with date code 8620 or later do not exhibit this problem.

3. If a RDVAL or a WRVAL is being executed and either the effective address to be validated or any data necessary to calculate that address reside in an invalid page, resulting in a page fault, the cpu and the mmu will get out of synchronization. This problem can be easily worked around by ensuring that no page fault occurs while the cpu is obtaining the effective address to be validated.

4. The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer length than the one specified by the instruction if the following conditions are BOTH true:
   1. Scaled indexing is used as an option with TOS or REG addressing mode (a very rare combination) for gen1 operand AND
   2. A write cycle is pending while the microcode is computing the Effective Address (EA routine) of the gen1 operand. A write cycle can only be pending if an instruction with RMW class has been executed prior to the above instructions and the write cycle has not been completed due to bus activities such as DMA.

   If the above conditions are BOTH true, then the instructions EXTSi and FFSi may generate wrong results. To bypass this problem for these TWO INSTRUCTIONS, the scaled indexing should not be used as an option with TOS or REG addressing mode for gen1 operand or if the combination is used, a dummy read cycle should be inserted before the above two instructions. For OTHER INSTRUCTIONS however, this problem is not harmful unless the read crosses a page boundary that was not supposed to be crossed, thus resulting in spurious page faults. If the page fault occurs it results in inefficincy that is not intentional.

   DATA SHEET CLARIFICATION
   ---

1. A 10K pull-up resistor is required on the SPC/AT line.

2. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with the falling edge of CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

3. The minimum clock frequencies for the NS32016-10 and NS32016-8/NS32016-6 are 6 Mhz and 4 MHz respectively, instead of 200 kHz as stated in the data sheet. At this frequency the maximum clock high voltage (on PHI1, PHI2) pins is Vcc instead of Vcc + 0.5 Volt.

4. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

5. The Output Leakage Current for output pins in TRI-STATE condition is 50/-50 microamps instead of 30/-20 microamps as stated in the data sheet.

USER INFORMATION

NS32016RT CPU, Rev S

June 1, 1987

ITEM 1
TITLE: ASYNCHRONOUS INTERRUPTS

DESCRIPTION
If /INT and /NMI are from asynchronous sources, they may cause metastability.

SUGGESTED WORKAROUND AND COMMENTS
/INT and /NMI should be synchronized with the rising edge of CTTL.

AFFECTED REVISIONS: N, M, R, S

ITEM 2
TITLE: PAGE FAULT on RDVAL, WRVAL

DESCRIPTION
If a RDVAL or a WRVAL is being executed and either the effective address to be validated or any data necessary to calculate that address reside in an invalid page, resulting in a page fault, the cpu and the mmu will get out of synchronization.

SUGGESTED WORKAROUND AND COMMENTS
It should be ensured that no page fault occurs while the cpu is obtaining the effective address to be validated.

AFFECTED REVISIONS: N, M, R, S

ITEM 3
TITLE: EXTSi, FFSi

DESCRIPTION
The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer length than the one specified by the instruction if the following conditions are BOTH true:

1. Scaled indexing is used as an option with TOS or REG addressing mode (a very rare combination) for gen1 operand AND
2. A write cycle is pending while the microcode is computing the Effective Address (EA routine) of the gen1 operand. A write cycle can only be pending if an instruction with RMW class has been executed prior to the above instructions and the write cycle has not been completed due to bus activities such as DMA.

SUGGESTED WORKAROUND AND COMMENTS
If the above conditions are BOTH true, then the instructions

EXTSi and FFSi may generate wrong results. To bypass this problem for these TWO INSTRUCTIONS, the scaled indexing should not be used as an option with TOS or REG addressing mode for gen1 operand or if the combination is used, a dummy read cycle should be inserted before the above two instructions. For OTHER INSTRUCTIONS however, this problem is not harmful unless the read crosses a page boundary that was not supposed to be crossed, thus resulting in spurious page faults. If the page fault occurs it results in inefficincy that is not intentional.

AFFECTED REVISIONS: N, M, R, S

ITEM 4
TITLE: A16-23 glitch

DESCRIPTION
In non-MMU systems, there is a possibility that A16-23 and output control signals /HBE, /ILO, and /DDIN will glitch during the narrow interval when address is changing to data (rising edge of PHI1 in T2).

SUGGESTED WORKAROUND AND COMMENTS
The glitch will not affect the cluster operation if an MMU is present, since valid address is available only after translation. The glitch is measured to be typically 5 ns wide if the AD outputs change from lots of 1s to lots of 0s (i.e. worst case, writing 0 to the address h'FFFFFF). In parts date coded 8712 or after, the peak of the glitch in the worst case does not exceeds 0.8 volts (Max Vih for a TTL gate) thus making the glitch not a problem. Note that the glitch is not critical if it occurs when the output is at high level. Further, in most systems the glitch on A16-23 and output control signals when the output is at low level is not a problem due to the timing of the glitch. In systems without an MMU it is recommended that A16-23 be latched if the glitch is to be avoided.

AFFECTED REVISIONS: S

DATA SHEET CLARIFICATION
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1. A 10K pull-up resistor is required on the SPC/AT line.

2. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with the falling edge of CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

3. The minimum clock frequencies for the NS32016-10 and NS32016-8/NS32016-6 are 6 MHz and 4 Mhz respectively, instead of 200 kHz as stated in the data sheet. At this frequency the

maximum clock high voltage (on PHI1, PHI2) pins is Vcc instead of Vcc + 0.5 Volt.

4. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

5. The Output Leakage Current for output pins in TRI-STATE condition is 50/-50 microamps instead of 30/-20 as stated in the data sheet.

USER INFORMATION

NS32016 CPU, Revision S

June 30, 1987

ITEM 1
TITLE: ASYNCHRONOUS INTERRUPTS

DESCRIPTION
If /INT and /NMI are from asynchronous sources, they may cause metastability.

SUGGESTED WORKAROUND AND COMMENTS
/INT and /NMI should be synchronized with the rising edge of CTTL.

AFFECTED REVISIONS: N, M, R, S

ITEM 2
TITLE: PAGE FAULT on RDVAL, WRVAL

DESCRIPTION
If a RDVAL or a WRVAL is being executed and either the effective address to be validated or any data necessary to calculate that address reside in an invalid page, resulting in a page fault, the cpu and the mmu will get out of synchronization.

SUGGESTED WORKAROUND AND COMMENTS
It should be ensured that no page fault occurs while the cpu is obtaining the effective address to be validated.

AFFECTED REVISIONS: N, M, R, S

ITEM 3
TITLE: EXTSi, FFSi

DESCRIPTION
The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer length than the one specified by the instruction if the following conditions are BOTH true:

1. Scaled indexing is used as an option with TOS or REG addressing mode (a very rare combination) for gen1 operand AND
2. A write cycle is pending while the microcode is computing the Effective Address (EA routine) of the gen1 operand. A write cycle can only be pending if an instruction with RMW class has been executed prior to the above instructions and the write cycle has not been completed due to bus activities such as DMA.

SUGGESTED WORKAROUND AND COMMENTS
If the above conditions are BOTH true, then the instructions

EXTSi and FFSi may generate wrong results. To bypass this problem for these TWO INSTRUCTIONS, the scaled indexing should not be used as an option with TOS or REG addressing mode for gen1 operand or if the combination is used, a dummy read cycle should be inserted before the above two instructions. For OTHER INSTRUCTIONS however, this problem is not harmful unless the read crosses a page boundary that was not supposed to be crossed, thus resulting in spurious page faults. If the page fault occurs it results in inefficincy that is not intentional.

AFFECTED REVISIONS: N, M, R, S

ITEM 4
TITLE: A16-23 glitch

DESCRIPTION
A16-23 and output control signals /HBE, /ILO, and /DDIN glitch during the narrow interval when address is changing to data, coincident with the rising edge of PHI1 in T2/Tmmu. The glitch is measured to be 5 ns wide. If these signals are at a low level, the measured peak of the glitch may exceed 0.8 volts. If the signals are at a high level, with the glitch they stay at a high valid TTL level (measured levels are always higher than 4.0 volts).

SUGGESTED WORKAROUND AND COMMENTS
The glitch will not affect the cluster operation if an MMU is present, since valid address is available only after translation when /PAV gets asserted in the Tmmu and approximately 40 ns after the glitch. To generate the worst case for the glitch, 0 should be written to the address h'FFFFFF and part be operated at 5.25 volts. In parts date coded 8712 or after, the peak of the glitch in the worst case does not exceed 0.8 volts (Max Vih for a TTL gate). In systems without an MMU using parts with earlier date codes than 8712, it is recommended that A16-23 be latched.

AFFECTED REVISIONS: S

DATA SHEET CLARIFICATION
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1. A 10K pull-up resistor is required on the SPC/AT line.

2. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with the falling edge of CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

3. The minimum clock frequencies for the NS32016-10 and NS32016-8/NS32016-6 are 6 MHz and 4 Mhz respectively, instead of 200 kHz as stated in the data sheet. At this frequency the

maximum clock high voltage (on PHI1, PHI2) pins is Vcc instead of Vcc + 0.5 Volt.

4. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

5. The Output Leakage Current for output pins in TRI-STATE condition is 50/-50 microamps instead of 30/-20 as stated in the data sheet.

USER INFORMATION

NS32C016 CPU, Revision E

March 26, 1987

1. The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer length than the one specified by the instruction if the following conditions are BOTH true:
   1. Scaled indexing is used as an option with TOS or REG addressing mode (a very rare combination) for gen1 operand AND
   2. A write cycle is pending while the microcode is computing the Effective Address (EA routine) of the gen1 operand. A write cycle can only be pending if an instruction with RMW class has been executed prior to the above instructions and the write cycle has not been completed due to bus activities such as DMA.

   If the above conditions are BOTH true, then the instructions EXTSi and FFSi may generate wrong results. To bypass this problem for these TWO INSTRUCTIONS, the scaled indexing should not be used as an option with TOS or REG addressing mode for gen1 operand or if the combination is used, a dummy read cycle should be inserted before the above two instructions. For OTHER INSTRUCTIONS however, this problem is not harmful unless the read crosses a page boundary that was not supposed to be crossed, thus resulting in spurious page faults. If the page fault occurs it results in inefficincy that is not intentional.

DATA SHEET CLARIFICATION
---

1. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

2. The minimum clock frequency for the NS32C016 is 4 Mhz instead of 200 Khz.

3. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

USER INFORMATION

NS32C016 CPU, Revision F

July 11, 1988

1. The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer length than the one specified by the instruction if the following conditions are BOTH true:
   1. Scaled indexing is used as an option with TOS or REG addressing mode (a very rare combination) for gen1 operand AND
   2. A write cycle is pending while the microcode is computing the Effective Address (EA routine) of the gen1 operand. A write cycle can only be pending if an instruction with RMW class has been executed prior to the above instructions and the write cycle has not been completed due to bus activities such as DMA.

   If the above conditions are BOTH true, then the instructions EXTSi and FFSi may generate wrong results. To bypass this problem for these TWO INSTRUCTIONS, the scaled indexing should not be used as an option with TOS or REG addressing mode for gen1 operand or if the combination is used, a dummy read cycle should be inserted before the above two instructions. For OTHER INSTRUCTIONS however, this problem is not harmful unless the read crosses a page boundary that was not supposed to be crossed, thus resulting in spurious page faults. If the page fault occurs it results in inefficincy that is not intentional.

DATA SHEET CHANGES/CLARIFICATIONS

1. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

2. The minimum clock frequency for the NS32C016 is 4 Mhz instead of 200 Khz.

3. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

4. The temperature range of the present parts is 0 to 70" C instead of -40 to 85" C.

5. The minimum value for tDIh is 3 nsec instead of 10.

USER INFORMATION

NS32CG16 CPU, Revision A

August 28, 1987

1. The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer length than the one specified by the instruction if the following conditions are BOTH true:

   I. Scaled indexing is used as an option with TOS or REG addressing mode for gen1 operand.

   II. A write cycle is pending while the microcode is computing the Effective Address of the gen1 operand. A write cycle can only be pending if an instruction with RMW class has been executed prior to the above instructions and the write cycle has not been completed due to bus activities such as DMA accesses.

   The instructions EXTSi and FFSi may also generate invalid results as a consequence of the above conditions. The results of the other instructions are always correct. The problem can be easily bypassed by avoiding the use of the scaled indexing option with either TOS or REG addressing modes for the gen1 operand, or by preceding any of the above instructions with an instruction that perfoms only memory read cycles.

2. Interrupts are not acknowledged during the execution of the EXTBLT instruction if the number of words in each line of the bit block is 1. The result is an increase of the interrupt latency, since interrupts are only recognized at the end of the instruction.

3. A spurious access of the stack with the /BPU signal asserted may occur when the EXTBLT instruction is restarted after being suspended by the occurrence of an interrupt. This can affect the operation of the DP8510 in case a pre-read (to load the DP8510 pipeline register) is performed at the beginning of each line. A possible solution to this problem is to qualify the /BPU signal with the memory select signal that enables the memory areas where BITBLT operations are allowed.

4. The /BPU signal is asserted at the end of any string instruction (e.g., MOVS,MOVST, CMPS, CMPST, SKPS, SKPST) if the PSR Z bit is set to 1. This problem can be avoided by placing a CMPQB 1,2 instruction (to clear the Z bit) before the string instruction.

DATA SHEET CLARIFICATION
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1. Instruction prefetches can occur during execution of the EXTBLT instruction. Therefore, the /BPU signal should be qualified with the data transfer status encoding (from ST0-3) in order to enable the external BITBLT unit.

2. The Acknowledging of /HOLD is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted.

USER INFORMATION

NS32CG16 CPU, Revision B

December 1, 1988

1. When executing the BBSTOD instruction, the resulting data written to the destination will be wrong under the following conditions:

   1. The shift value is greater than zero.
   2. The number of words per line is greater than 2.
   3. The CPU clock frequency is greater than 7.5 MHz.

   The following code sequence may be used as a workaround:

```
setcfg [m]      ;divide clock frequency by 2
bbstod
setcfg [ ]      ;divide clock frequency by 1
```

   This problem affects parts date coded 5622 and earlier.

2. The minimum clock frequency is 3.75 MHz.

3. At the end of execution of an EXTBLT instruction, the /BPU signal will go inactive before the last destination write by the BPU if a combination of DMA or wait cycles adds more than 16 cycles after the the next to last destination write and before or during the last source and destination reads.

   As a workaround, external hardware can be used to extend the /BPU signal through the last destination write cycle. For those users using the the BPU interface shown in NS32CG16 Graphics App Note 2 "Simple Embedded Control NS32CG16 System", a D flip flop can be inserted in the /BPUSTAT signal path as shown below.

4. The traps DVZ, during the execution of DEI, and ILL, during the execution of BICPSR, BISPSR and LPR, will not execute properly if there are more than 14 consecutive wait states in a bus cycle or more than 9 wait states when combined with DMA activity.

5. For the undefined opcodes 111 and 110 in format 8, the CPU will lock up if the REG value is 1XX or 010. The CPU will correctly trap UND for the other values of REG.

DATA SHEET CLARIFICATIONS

The following clarifications relate to the July 1988 NS32CG16 data sheet.

1. The power save mode should not be used to reduce the clock frequency below the minimum clock frequency required by the CPU.

2. During DMA cycles, /WAIT1-2 should be kept inactive unless they are monitored by the DMA controller.

3. All the timing specifications given in the AC specs refer to 0.8V or 2.0V on the rising or falling edges of CTTL, when the capacitive loading of CTTL is 100pF, unless specifically stated otherwise. The timing specifications refer to 0.8V or 2.0V on all the TTL input and output signals, unless specifically stated otherwise.

   The voltage thresholds in figures 4-2 and 4-3 should be changed to 2.0 and 0.8 volts on the rising and falling edges respectively. Figure 4-2 now refers to TTL output signals.

4. The maximum capacitive loading of OSCOUT, including stray capacitance, is given in Table 3.1 when the NS32CG16's internal oscillator is driven with a crystal. The OSCOUT pin should be left unconnected, with no more than 5pF of capacitive loading, if a single phase clock source is used.

5. The NS32CG16 slave protocol specification is being clarified to allow for the use of custom slave FPUs other than the NS32081 and NS32381. The following 15MHz AC specs apply when the NS32CG16 is connected to custom slaves only, not the NS32081 or NS32381 FPUs.

   An input spec, tSPCh (SPC Hold Time), is added.

   tSPCh is 0ns after the RE CTTL.

   tSPCw (SPC Pulse Width from Slave) is deleted.

   tSPCd (SPC Pulse Delay from Slave) is 2 tCTp after FE CTTL T4.

   tSPCnf (SPC Output non-forcing) is tCTp+8 ns after FE CTTL T4.

6. The logic value of the status pins, ST0-ST3, is undefined during DMA activity.

DATA SHEET CHANGES

The following changes relate to the July 1988 NS32CG16 data sheet.

1. /INT no longer needs to be synchronized with CTTL to minimize the possibility of metastable states. The /INT signal setup spec, tINTs is dropped from the data sheet.

2. A new spec, tALfr (Address Bits 0-15 floating during read), is added to the data sheet.

   tALfr @15MHz is 5 ns MIN, 28 ns MAX after RE CTTL T2.

3. The following 15MHz specs are changed.

   tCTr is 0 ns. MIN

   tCTf is 0 ns. MIN

   tCLh is 18 ns. MIN

   tCLw is 21 ns. MIN

   tRDia is 0 ns. MIN

   tWRia is 0 ns. MIN

   tTSOa is 12 ns. MAX

   tSPCs is 10 ns. MIN

USER INFORMATION

NS32032 CPU Revision F1

October 28, 1985

1. In executing the RETT or RETI instruction, the CPU will sometimes read the MOD register value from the wrong address, and also with incorrect byte order and/or missing bytes. The incorrect address will be offset by a small amount (+/- 3 bytes) from the correct address. The instruction continues by attempting to read the SB value from the incorrect address in the MOD register. This problem is associated with a specific set of timing sequences on the bus, involving HOLD/HLDA DMA and/or WAIT states. It can be bypassed by aligning the RETT instruction so that it can be fetched in one memory cycle, and disaligning the stack containing the return address so that the CPU must pop the return address in two (or more) memory cycles. Doing both of these together prevents the sequences that lead to this failure. This also applies to all previous revisions.

2. Converting a double-precision floating-point immediate value to a one-byte or two-byte integer (e.g. TRUNCLB 1.0,TOS) brings the CPU and FPU to a mutual deadlock, requiring a Reset. The problem is within this CPU revision and all previous revisions. (The instruction forms in question are probably useless, but could occur due to a programming error.)

3. The instructions CMPF and CMPL, if they generate a Trap(FPU), may cause the CPU to read the trap's interrupt descriptor from an address other than INTBASE + h'0C, or they may bring the CPU to an internal deadlock, requiring a reset. The bad address will be in the range INTBASE + h'2000 through INTBASE + h'327FC, depending on the exact encoding of the most significant 16 bits of the Basic Instruction field of the instruction. Note that the only condition under which these instructions will generate Trap(FPU) is when they are given a Reserved operand value. See the Instruction Set Manual, Section 3.3. This also applies to all previous revisions.

   MMU instructions can also trigger the above problem if a Rev. K1 or earlier MMU is used and DMA requests are occurring using the HOLD pin. This, however, is only one effect of an MMU bug which would be fatal regardless.

4. Shift instructions of the form:

```
LSHW    any-source,TOS
LSHD    any-source,TOS
ASHW    any-source,TOS
ASHD    any-source,TOS
```

   may misinterpret the sign and magnitude of the first operand, causing an incorrect shift direction and count. Use 0(SP) instead of TOS to bypass this problem.

5. The floating-point instructions MOVBF and MOVBL do not execute correctly. The CPU may send an incorrect integer value to the FPU for conversion. To bypass this, convert the integer byte to any larger size (using, for example, the MOVXBD instruction) and then convert the larger size value.

6. DMA requests made to the CPU on the HOLD pin may cause the CPU to lock up if they are made during the T1, T3 or Ti CPU states. HOLD requests should be synchronized to the rising edge of PHI1,should be asserted only during T2 or T4 and should be inhibited during slave operations.

7. The DEIi instruction may generate invalid results when the quotient part overflows by more than one bit. In this case the quotient should be truncated and the remainder should have the correct value.

8. There is a potential for a problem at 10 Mhz when the CPU addresses the 128 bytes residing in the virtual address range FFFF80 to FFFFFF. The problem manifests itself in changing of the address bit 22 (A22) from a '1' to a '0' while ADS is still low. This problem can be worked around by not addressing the FFFF80..FFFFFF address range.

9. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

10. A very small number of CPUs with date code prior to 8540 may malfunction at high temperature and 10 MHz when 'register' addressing mode is specified. If the problem occurs the CPU selects a wrong operand address. The problem does not occur on devices with a more recent date code or shipped directly by National after 10-5-85.

DATA SHEET CHANGES / CLARIFICATIONS
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1. Starting with Revision C of the NS32032, it is necessary to pull pin 61 high using a 4.7K resistor. This pin must no longer be attached to ground.

2. An external 10K ohm resistor to VCC is required on the SPC/AT line. This also applies to all previous revisions.

3. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

4. The minimum clock frequency for the 32000 family processors, CPU, MMU, and FPU, is 4 Mhz instead of 200 Khz as stated in the data sheets.

USER INFORMATION

NS32032 CPU Revision G

March 26, 1987

1. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

2. If a RDVAL or a WRVAL is being executed and either the effective address to be validated or any data necessary to calculate that address reside in an invalid page, resulting in a page fault, the cpu and the mmu will get out of synchronization. This problem can be easily worked around by ensuring that no page fault occurs while the cpu is obtaining the effective address to be validated.

3. The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer lenght than the one specified by the instruction if the following conditions are BOTH true:
   1. Scaled indexing is used as an option with TOS or REG addressing mode (a very rare combination) for gen1 operand AND
   2. A write cycle is pending while the microcode is computing the Effective Address (EA routine) of the gen1 operand. A write cycle can only be pending if an instruction with RMW class has been executed prior to the above instructions and the write cycle has not been completed due to bus activities such as DMA.

   If the above conditions are BOTH true, then the instructions EXTSi and FFSi may generate wrong results. To bypass this problem for these TWO INSTRUCTIONS, the the scaled indexing should not be used as an option with TOS or REG addressing mode for gen1 operand or if the combination is used, a dummy read cycle should be inserted before the above two instructions. For OTHER INSTRUCTIONS however, this problem is not harmful unless the read crosses a page boundary that was not supposed to be crossed, thus resulting in spurious page faults. If the page fault occurs it results in inefficincy that is not intentional.

DATA SHEET CHANGES / CLARIFICATIONS
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1. Starting with Revision C of the NS32032, it is necessary to pull pin 61 high using a 4.7K resistor. This pin must no longer be attached to ground.

2. An external 10K ohm resistor to VCC is required on the SPC/AT line. This also applies to all previous revisions.

3. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with the falling edge of CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

4. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

5. The minimum clock frequencies for the NS32032-10 and NS32032-8/NS32032-6 are 6 Mhz and 4 Mhz respectively, instead of 200 Khz as stated in the data sheet. At this frequency the maximum clock high voltage (on PHI1, PHI2 Pins) is Vcc instead of Vcc + 0.5 Volt.

USER INFORMATION

NS32032 CPU Revision H

March 26, 1987

1. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

2. If a RDVAL or a WRVAL is being executed and either the effective address to be validated or any data necessary to calculate that address reside in an invalid page, resulting in a page fault, the cpu and the mmu will get out of synchronization. This problem can be easily worked around by ensuring that no page fault occurs while the cpu is obtaining the effective address to be validated.

3. The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer lenght than the one specified by the instruction if the following conditions are BOTH true:
   1. Scaled indexing is used as an option with TOS or REG addressing mode (a very rare combination) for gen1 operand AND
   2. A write cycle is pending while the microcode is computing the Effective Address (EA routine) of the gen1 operand. A write cycle can only be pending if an instruction with RMW class has been executed prior to the above instructions and the write cycle has not been completed due to bus activities such as DMA.

   If the above conditions are BOTH true, then the instructions EXTSi and FFSi may generate wrong results. To bypass this problem for these TWO INSTRUCTIONS, the the scaled indexing should not be used as an option with TOS or REG addressing mode for gen1 operand or if the combination is used, a dummy read cycle should be inserted before the above two instructions. For OTHER INSTRUCTIONS however, this problem is not harmful unless the read crosses a page boundary that was not supposed to be crossed, thus resulting in spurious page faults. If the page fault occurs it results in inefficincy that is not intentional.

DATA SHEET CHANGES / CLARIFICATIONS
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1. Starting with Revision C of the NS32032, it is necessary to pull pin 61 high using a 4.7K resistor. This pin must no longer be attached to ground.

2. An external 10K ohm resistor to VCC is required on the SPC/AT line. This also applies to all previous revisions.

3. If the HOLD signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with the falling edge of CTTL to minimize the possibility of metastable states. The CPU provides only one synchronization stage to minimize the HLDA latency. This is to avoid speed degradations in cases of heavy HOLD activity (i.e. DMA controller cycles interleaved with CPU cycles.)

4. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

5. The minimum clock frequencies for the NS32032-10 and NS32032-8/NS32032-6 are 6 Mhz and 4 Mhz respectively, instead of 200 Khz as stated in the data sheet. At this frequency the maximum clock high voltage (on PHI1, PHI2 Pins) is Vcc instead of Vcc + 0.5 Volt.

USER INFORMATION

NS32c032 CPU Revision A

March 26, 1987

1. If a RDVAL or a WRVAL is being executed and either the effective address to be validated or any data necessary to calculate that address reside in an invalid page, resulting in a page fault, the cpu and the mmu will get out of synchronization. This problem can be easily worked around by ensuring that no page fault occurs while the cpu is obtaining the effective address to be validated.

2. The instructions LSHi, ASHi, ROTi, MOVXBW, MOVXiD, MOVZBW, MOVZiD, INSSi, MOVif, EXTSi, and FFSi may cause the read of the gen1 operand to be of a longer length than the one specified by the instruction if the following conditions are BOTH true:
   1. Scaled indexing is used as an option with TOS or REG addressing mode (a very rare combination) for gen1 operand AND
   2. A write cycle is pending while the microcode is computing the Effective Address (EA routine) of the gen1 operand. A write cycle can only be pending if an instruction with RMW class has been executed prior to the above instructions and the write cycle has not been completed due to bus activities such as DMA.

   If the above conditions are BOTH true, then the instructions EXTSi and FFSi may generate wrong results. To bypass this problem for these TWO INSTRUCTIONS, the scaled indexing should not be used as an option with TOS or REG addressing mode for gen1 operand or if the combination is used, a dummy read cycle should be inserted before the above two instructions. For OTHER INSTRUCTIONS however, this problem is not harmful unless the read crosses a page boundary that was not supposed to be crossed, thus resulting in spurious page faults. If the page fault occurs it results in inefficincy that is not intentional.

DATA SHEET CHANGES / CLARIFICATIONS
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1. If INT and NMI are from asynchronous sources, they should be synchronized with the rising edge of CTTL to minimize the possibility of metastable states.

2. Acknowledging /HOLD signal is on a cycle by cycle basis. Therefore, it is possible to have /HLDA active when an interlocked operation is in progress. In this case /ILO remains low and the interlocked instruction execution continues only after /HOLD is de-asserted to the CPU.

DATA SHEET CHANGES/CLARIFICATIONS
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1. The /MC should be detected as valid if it holds its value for two consecutive clock cycles.

2. If the NS32332 is executing an instruction which results in a jump and thus a queue flush, and its BIU is prefetching via bursting, the burst will be terminated before the address reaches an appropriate boundary (i.e. 16 byte boundary in the 32 bit bus mode). In this case /BOUT will be deasserted indicating an internal termination of the burst.

3. In the NS32332 data sheet, there is no MAX specified for tBERh. The state after detecting a Bus Error in T4 state is a Ti. The Bus Error should be deasserted to the CPU at the latest in the beginning of the cycle following this Ti cycle.

4. The opcodes for the LCR and SCR instructions are incorrect as shown in the data sheet. The correct opcodes are 0010 and 0011 for LCR and SCR, respectively.

5. The Max for AC parameter tDr has been changed to 38 and 50 ns at 15 and 10 Mhz respectively. This parameter is measured relative to the PHI1 RE of the state T3.

6. Output leakage current for AD pins (AD pins in TRI-STATE condition) is -150 microamps and +1 mA when Vout is at 0.4 volts and Vcc respectively. For the remaining output pins the output leakage current is -60 and +60 microamps when Vout is at 0.4 volts and Vcc respectively.

7. The maximum for the active supply current (Icc max) is 600 mA.

8. The maximum for the Vol is 0.55 volts.

USER INFORMATION
NS32332 CPU Revision D
February 15, 1987

DATA SHEET CHANGES/CLARIFICATIONS
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1. The /MC should be detected as valid if it holds its value for two consecutive clock cycles.

2. If the NS32332 is executing an instruction which results in a jump and thus a queue flush, and its BIU is prefetching via bursting, the burst will be terminated before the address reaches an appropriate boundary (i.e. 16 byte boundary in the 32 bit bus mode). In this case /BOUT will be deasserted indicating an internal termination of the burst.

3. In the NS32332 data sheet, there is no MAX specified for tBERh. The state after detecting a Bus Error in T4 state is a Ti. The Bus Error should be deasserted to the CPU at the latest in the beginning of the cycle following this Ti cycle.

4. The opcodes for the LCR and SCR instructions are incorrect as shown in the data sheet. The correct opcodes are 0010 and 0011 for LCR and SCR, respectively.

5. The Max for AC parameter tDr has been changed to 38 and 50 ns at 15 and 10 Mhz respectively. This parameter is measured relative to the PHI1 RE of the state T3.

6. As of revision D, the NS32c201 should be used to provide the PHi clocks of the NS32332. This is due to the tightening of the non-overlap timing specification (tnOVL) for the NS32332. The NS32c201 provides the required PHi signals for the NS32332.

7. Output leakage current, Io(OFF), for AD pins (AD pins in TRI-STATE condition) is as follows:
   -150 microamps when Vout = 0.4 volts
   +1 mA when Vout = Vcc
   +350 microamps when Vout = 2.4 volts
   For the remaining output pins the output leakage current is -60 and +60 microamps when Vout is at 0.4 volts and Vcc respectively.

8. The maximum for the active supply current (Icc max) is 600 mA.

9. The minimum Vch is 4.25 volts when the part is operating in the 4.5-4.75 voltage range (10% tolerance part).

ERRATA SHEET
NS32532 CPU Revision A1
January 14, 1988

1. Hardware Debug facilities, Breakpoint on Address Compare and DBG input, are not functional. However, Breakpointing on Program Counter is functional (1126, 1128, 1142, 1232, 1240, 1241, 1243).

2. /NMI input should be kept inactive while /RST is being low (1135).

3. LPRw CFG should be used to invalidate the instruction cache. The CINV instruction does not work correctly (1159, 1196).

4. /RDY input is sampled during slave cycles. /RDY must be kept low during slave cycles (as noted in the data sheet) to bypass this problem (1187).

5. The minimum Vih level for the CLK input should be 2.5 volts instead of 2.0 volts as specified in the data sheet (1192).

6. The CPU will hang if an FFSi instruction is being executed and an abort is generated on accessing the offset field. This problem can be bypassed by placing the offset field in a register (1197).

7. The instructions RDVAL and WRVAL should be used with valid pages only. If the V bit in the PTE is 0, the F bit gets set regardless of the value of PL bits. Furthermore, these instructions execute regardless of the value of MCR.AO bit. If the above solution is unacceptable, then RDVAL and WRVAL should be performed in software (1203, 1205).

8. Overflow trap may be generated erroneously when the DEI instruction is excecuted. Clearing the PSR.V bit before execution of the DEI instruction will bypass this problem (1206).

9. Immediate mode addressing should not be used for the source operand of the CHECKi (i=b or w) instruction (1207).

10. Instruction fetch bursts should not be stopped until completed as flagged by the CPU /BOUT or the 16-byte boundary (1210).

11. The result of an FPU instruction may be erroneous in one of the following cases:
    a) the first operand is an immediate long AND the second operand has a memory relative or external addressing modes or uses indexing.
    b) the second operand has a memory space (register relative) addressing mode AND Bus Error or Abort may be generated on the operand access.
    The above combinations should be avoided for the FP instructions to work correctly. Furthermore, case b may cause

the CPU to halt (1211, 1216).

12. During execution of SBITI and CBITI instructions, an MMU transaction can occur between the interlocked read and write portions (note that the /ILO will be removed during the MMU transaction). If this causes any problem, then the above instructions should be performed on pages that have been modified (PTE.M bit is set) (1212).

13. In rare circumstances, instructions MOVM, CMPM, MOVS(T), SKPS(T), CMPS(T) may bring the CPU to a halt. These instructions should not be used with this revision of the CPU (1213).

14. /IODEC should not be activated with 8-bit bus mode. However, there are no restrictions on /IODEC activation if the DCR.SI bit is set (disabling the instructions' execution overlap) (1214).

15. The CPU may hang if instructions SMR or 'SPRi CAR,dest' are executed. To bypass this problem, the followings must be done:
    - Execute these instructions with register destination
    - Before executing these instructions invalidate the instruction cache via LPRD CFG bit
    - align the SMR to 16-byte boundary
    - After the instruction insert three NOP's (1215).

16. There is a chance that the BSR instruction may execute twice. The instruction JSR should be used instead of BSR (1217).

17. Bcond and ACBi instructions may branch to the wrong address. To bypass this problem both of the following conditions must be met:
    1) Branch prediction should be turned off via DCR.BCP bit.
    2) Every BR instruction must be preceded by at least three sequential instructions (NOPs can be used if necessary). This way it is guaranteed that the combination of BR preceded by a Bcond is not present in the pipeline (1218).

18. If an instruction prefetch from the target of the BR, BSR, or Bcond instructions is aborted due to Abort or /BER, the outcome is unpredictable. To bypass this problem, JSR should be used instead of BSR, Branch prediction should be disabled via DCR.BCP bit, and BR instructions should be replaced by Bcond with the condition always true (1219).

19. The CPU may hang if the /BER input is asserted. The /BER input should be pulled to Vcc to bypass this problem. Other inputs such as /DBG or /NMI should be used for bus error indication (1224, 1226, 1230, 1231).

20. The PSR.U bit may not be updated upon execution of the RETT instruction if the Direct Exception mode is enabled. This problem can be bypassed if a serializing instruction is executed prior to execution of the RETT instruction (1228).

21. The instructions LPRi and SPRi should not be used with the operands DSR and BPC registers in the user mode. This problem affects the use of debug facilities in the user mode (1238).

22. The following restrictions must be observed if the instructions EXTi and INSi are used:
    - Insert a NOP before these instructions
    - Avoid Abort, Bus-error, or /IOINH on the 'src' of the INSi instruction (1242 , 1252 ,1255).

23. If /BER or abort is generated when fetching INDEXi instruction, the processor may halt. To bypass this problem the INDEXi accum,lenght,index instruction should be replaced with the sequence:
    ```
    MULi (length+1), accum
    ADDi index, accum (1253).
    ```

24. Non-restartable abort or bus-error on instructions using scaled index mode may produce erroneous result after the instruction returns from the exception routine. To bypass the problem a NOP should be inserted before the instructions with the following conditions:
    - Source of the instruction uses scaled index mode
    - Destination of the instruction is a RMW class
    - Destination of the instruction is a register

    OR
    - Source of the instruction uses scaled index mode
    - and destination of the instruction is a register
    - and source of the instruction uses the destination register for effective address calculation (1256).

DATA SHEET CHANGES / CLARIFICATIONS
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1. If /BER is issued to the CPU during a burst transfer or a split bus cycle due to 8/16 bit bus, the CPU continues to bring in the remaining transactions. However, the CPU will ignore the remaining transactions and Bus Error routine will be entered correctly.

2. With the next revision of the NS32532, the branch prediction mechanism will predict forward branches as taken for the instructions BLE and BNE.

3. The following changes are made to the AC timing specification:
   tRDYs is 15, 18, and 22 ns at 30, 25, and 20 Mhz respectively.
   tSPCa is 12, 15, and 19 ns at 30, 25, and 20 Mhz respectively.
   tSPCia is 12, 15, and 19 ns at 30, 25, and 20 Mhz respectively.

ERRATA SHEET Ver 7.0
NS32532 CPU Revision A2
August 11, 1988

1. Hardware Debug facilities, Breakpoint on Address Compare and DBG input, are not functional. However, Breakpointing on Program Counter is functional (1126, 1128, 1142, 1232, 1240, 1241, 1243, 1249).

2. The minimum Vih level for the CLK input should be 2.5 volts instead of 2.0 volts as specified in the data sheet (1192).

3. The instructions RDVAL and WRVAL will abort if the PTE1.v bit is 0 (similar to the NS32082 behaviour) (1225).

4. The instructions LPRi and SPRi should not be used with the operands DSR and BPC registers in the user mode. This problem affects the use of debug facilities in the user mode (1238).

5. The instructions EXTi and INSi may produce wrong results. To bypass this problem, both of the following restrictions must be observed:
   - Insert a NOP before these instructions
   - Avoid Abort, Bus-error, or /IOINH on the 'src' of the INSi instruction (/IOINH can be avoided by using a register for the source). (1242, 1252, 1255).

6. After asserting the /BER, /BRT should not be asserted on the same operand transfer (1251).

7. If /BER or abort is generated when fetching INDEXi instruction, the processor may halt. To bypass this problem the INDEXi accum,lenght,index instruction should be replaced with the sequence:

```
        MULi (length+1), accum
        ADDi index, accum (1253).
```

8. If the instructions LMR, SMR, CINV, RDVAL, WRVAL, LPR CAR, LPR DCR, and SPR CAR follow the execution of RESTORE or EXIT instructions, they will exhibit erroneous behaviour. To bypass this problem either of the following code sequences should be executed before the problematic instructions and after the last RESTORE or EXIT in the abort, interrupt, and bus-error handlers.
   Either:

```
        TBITi $0,TOS
```

   Or:

```
        SFSb     TOS  ; push original F bit onto stack
        TBITb $0,TOS  ; restore F bit while bypassing the bug
        ADJSP $-1     ; restore stack (1254)
```

9. Non-restartable abort or bus-error on instructions using scaled index mode may produce erroneous result after the instruction returns from the exception routine. To bypass the problem a NOP should be inserted before the instructions with the

following conditions:
- Source of the instruction uses scaled index mode
- Destination of the instruction is a RMW class
- Destination of the instruction is a register

OR
- Source of the instruction uses scaled index mode
- destination of the instruction is a register
- source of the instruction uses the destination register for effective address calculation

Another workaround is addition of a NOP prior to all instructions that use scaled indexing with the exception of CASEi instruction (1256).

10. Floating-point restrictions:

    a. If an Abort or Bus Error occurs during the access of a floating point operand, a write to an undefined address may result. (1258, 1267).

    b. A TRAP issued for a floating-point instruction followed by an instruction that reads an operand from memory may cause unpredictable results. (1268).

    The first problem can be avoided by keeping floating point operands in registers or, by making sure that an Abort or a Bus Error will not occur during the operand access.

    The second problem can be avoided by inserting a NOP after each floating point instruction.

11. Abort or Bus-error on fetching the displacement of the destination operand of the instruction SPRi CAR,gen may cause unpredictable results. The destination operand should be placed in a register to bypass this problem (1260).

12. The PSR may get corrupted if the DEI instruction is executed with the destination operand in the I/O space. If the DEI instruction is executed with its destination operand in the I/O space (IODEC is asserted to the processor), a serializing instruction should be executed before the DEI instruction (1263).

13. There is a remote possibility that Bus Error on data access immediately following an MMU access causes the CPU to enter the halt state. This problem can be bypassed by assertin /BER together with /IODEC.
    (The setup time for /IODEC must be met).

14. The second vector read during a cascaded interrupt acknowledge should not return a value in the range of 63-255.

15. Wrong OVF trap may be generated when executing MULD instruction.

16. An operand access of class RMW immediately following a FLAG instruction may cause unpredictable results. This problem can be bypassed by inserting a NOP after each FLAG instruction.

17. Bus error on write accesses or on MMU accesses can cause unpredictable results. (1276).

18. There is a remote possibility that Power-on Reset is not accepted. This problem can be easily avoided by asserting the /RST signal again after power-on. (1278).

19. Extra trace trap may happen in case INT or DBG are detected during execution of RETT from the trace handler (or any other instruction which sets the T bit in the PSR).

DATA SHEET CHANGES / CLARIFICATIONS

The following changes should be made to the October 1987 NS32532 data sheet.

1. If /BER is issued to the CPU during a burst transfer or a split bus cycle due to 8/16 bit bus, the CPU continues to bring in the remaining transactions. However, the CPU will ignore the remaining transactions and Bus Error routine will be entered correctly.

2. With the next revision of the NS32532, the branch prediction mechanism will predict forward branches as taken for the instructions BLE and BNE.

3. Software must clear all bits in the DSR (RD included) when appropriate (Data Sheet Section 2.1.6).

4. When a debug condition is detected during execution of an instruction, the /BP signal is asserted at the beginning of the next instruction. If the instruction is aborted, /BP may or may not be asserted. (Data sheet section 3.3.2).

5. BCLK and /BCLK should see a capacitive load of at least 50 pf. The CPU requires this in order to meet the timing values specified in the data sheet. (section 4.4.2.1).

6. The custom slave instructions CATST0 and CATST1 are not supported. (Data sheet page 23).

7. /SDONE and /FSSR should be pulled high with 10k resistors.

8. Floating-point instructions are not interruptible. Therefore, the PSR I-flag is not transferred to the FPU. (Data sheet section 3.1.4.1).

9. If /BER is asserted during the ICU read cycle of a RETI instruction, a fatal bus error results and the HALT state is entered. (data sheet section 3.2.6).

10. A burst transfer or a regular multicycle transfer is not stopped by the assertion of /BER. However, the data read after the assertion of /BER is ignored.

11. CIOUT, /IOINH and U/S are not floated during HOLD acknowledge. Therefore, the timing parameters tUSf, tUSnf, tCOf, tCOnf, tIOIf and tIOInf should be eliminated.

12. The following changes are made to the AC timing specification:

    tBCp Max is 100 ns at 30, 25, and 20 Mhz.

    tCONFia is referenced to BCLK RE in T1 or Ti.

    tADSw Min is 10, 12, and 15 ns at 30, 25, and 20 Mhz respectively.

    tSPCa is 12, 15, and 19 ns at 30, 25, and 20 Mhz respectively.

    tSPCia is referenced to BCLK RE in Ti, T1, or T2.
    tSPCia is 12, 15, and 19 ns at 30, 25, and 20 Mhz respectively.

    tBOUTa is referenced to BCLK RE in T2.

    tBOUTia is referenced to BCLK RE in last T2B, T1, or Ti.

    tRDYs is 15, 18, and 22 ns at 30, 25, and 20 Mhz respectively.

    tIODs is 14, 17, and 21 ns at 30, 25, and 20 Mhz respectively.

ERRATA SHEET
NS32532 CPU Revision B
April 19, 1988

1. Limitations on the Debug Features

   a. An address compare condition on a string instruction will only be served at the end of the instruction, and only if no exception has occurred during the instruction (i.e., interrupt, abort, etc.). (1275).

   b. An address compare condition will not be detected on the operands of a CMPf instruction.

2. Bus error on write accesses or on MMU accesses can cause unpredictable results. (1276).

3. There is a remote possibility that Power-on Reset is not accepted. This problem can be easily avoided by asserting the /RST signal again after power-on. (1278).

DATA SHEET CHANGES / CLARIFICATIONS

The following changes should be made to the October 1987 NS32532 data sheet.

1. If /BER is issued to the CPU during a burst transfer or a split bus cycle due to 8/16 bit bus, the CPU continues to bring in the remaining transactions. However, the CPU will ignore the remaining transactions and Bus Error routine will be entered correctly.

2. Branch instructions BLE and BNE are always predicted as taken. (Data sheet section 3.1.3.1.).

3. Software must clear all bits in the DSR (RD included) when appropriate (Data Sheet Section 2.1.6).

4. When a debug condition is detected during execution of an instruction, the /BP signal is asserted at the beginning of the next instruction. If the instruction is aborted, /BP may or may not be asserted. (Data sheet section 3.3.2).

5. BCLK and /BCLK should see a capacitive load of at least 50 pf. The CPU requires this in order to meet the timing values specified in the data sheet. (section 4.4.2.1).

6. The custom slave instructions CATST0 and CATST1 are not supported. (Data sheet page 23).

7. /SDONE and /FSSR should be pulled high with 10k resistors.

8. Floating-point instructions are not interruptible. Therefore, the PSR I-flag is not transferred to the FPU. (Data sheet section 3.1.4.1).

9. If /BER is asserted during the ICU read cycle of a RETI instruction, a fatal bus error results and the HALT state is entered. (data sheet section 3.2.6).

10. A burst transfer or a regular multicycle transfer is not stopped by the assertion of /BER. However, the data read after the assertion of /BER is ignored.

11. CIOUT, /IOINH and U/S are not floated during HOLD acknowledge. Therefore, the timing parameters tUSf, tUSnf, tCOf, tCOnf, tIOIf and tIOInf should be eliminated.

12. The following changes are made to the AC timing specification:

    tBCp Max is 100 ns at 30, 25, and 20 Mhz.

    tCONFia is referenced to BCLK RE in T1 or Ti.

    tADSw Min is 10, 12, and 15 ns at 30, 25, and 20 Mhz respectively.

    tSPCa is 12, 15, and 19 ns at 30, 25, and 20 Mhz respectively.

    tSPCia is referenced to BCLK RE in Ti, T1, or T2.
    tSPCia is 12, 15, and 19 ns at 30, 25, and 20 Mhz respectively.

    tBOUTa is referenced to BCLK RE in T2.

    tBOUTia is referenced to BCLK RE in last T2B, T1, or Ti.

    tRDYs is 15, 18, and 22 ns at 30, 25, and 20 Mhz respectively.

    tIODs is 14, 17, and 21 ns at 30, 25, and 20 Mhz respectively.

ERRATA SHEET Ver 2.0
NS32532 CPU Revision B2
September 5, 1988

1. Extra trace trap may happen in case INT or DBG are detected during execution of RETT from the trace handler (or any other instruction which sets the T bit in the PSR). (1310).

2. RDVAL and WRVAL instructions may produce a wrong result if the translation information for page FFFFF is in the TLB. (1311).

   Bypass: Add the following instructions before any RDVAL/WRVAL instruction.

   ```
   LMR IVAR0,H'FFFFF000
   LMR IVAR1,H'FFFFF000
   ```

   If the page FFFFF is referenced only in supervisor mode, the second instruction above is not needed.

3. The timing parameter tSTv is 10 and 9 nsec instead of 8 and 7 at 25 and 30 MHz respectively.

4. A deadlock may occur when the following sequence of instructions is executed:

   - Instruction N is a floating point long instruction with gen1 or gen2 in memory.

   - Instruction N-1 is a floating point instruction from format 11 whose gen1 in not TOS or IMMEDIATE and gen2 is an FPU register.

   - Instruction N-i has a memory destination. (i is theoretically 2 or more, practically 2). (1306).

   Bypass: Add a NOP instruction before every floating point long instruction with gen1 or gen2 in memory.

5. An integer instruction that follows a floating point instruction from format 11 whose gen2 is an FPU register and gen1 is not TOS or IMMEDIATE, may be executed even if the floating point instruction traps. The FPU trap will be handled only after the execution of the integer instruction.
   This may happen only when the PF bit in the CFG register is set to 1. (1302).

   Bypass: Add a NOP instruction between every floating point instruction that satisfies the above conditions and an integer instruction, or clear the PF bit in CFG.

6. A deadlock may occur during the execution of one of the following instructions when the destination operand crosses a page boundary and an abort occurs in the access of the portion

of the operand residing in the top page. (1312).

- Floating point instruction with long destination operand.

- MEIi or DEIi

Bypass: Make sure that the destination operand is either aligned or, if it crosses a page boundary, the top page is valid.

DATA SHEET CHANGES / CLARIFICATIONS

The following changes should be made to the August 1988 NS32532 data sheet.

1. The BF bit in the DCR register is not supported any longer and it should be set to 0.

2. The timing parameter tCASh is specified relative to the rising edge of BCLK instead of the falling edge.

1. Extra trace trap may happen in case INT or DBG are detected during execution of RETT from the trace handler (or any other instruction which sets the T bit in the PSR). (1310).

2. The floating point pipelined mode is not functional. This problem can be avoided by setting the PF bit in the CFG register to 0.

3. RDVAL and WRVAL instructions may produce a wrong result if the translation information for page FFFFF is in the TLB. (1311).

   Bypass: Add the following instructions before any RDVAL/WRVAL instruction.

   ```
   LMR IVAR0,H'FFFFF000
   LMR IVAR1,H'FFFFF000
   ```

   If the page FFFFF is referenced only in supervisor mode, the second instruction above is not needed.

4. The timing parameter tSTv is 10 and 9 nsec instead of 8 and 7 at 25 and 30 MHz respectively.

5. A deadlock may occur during the execution of one of the following instructions when the destination operand crosses a page boundary and an abort occurs during the access of the portion of the operand residing in the top page. (1312).

   - Floating point instruction with long destination operand.

   Bypass: Software: Make sure that the destination operand is either aligned or, if it crosses a page boundary, the top page is valid.

   Hardware: There is a hardware fix which utilizes a GAL device and two logic gates that forces a floating point exception if there is going to be a fault. This has been tested in a customer design and information can be obtained from NSC Series 32000 Applications.

6. RDVAL and WRVAL may produce a wrong result if address bit A31 is high and Protection Level is not OK. (1319)

   Bypass: Don't use RDVAL/WRVAL for the addresses with A31 high.

DATA SHEET CHANGES / CLARIFICATIONS

The following changes should be made to the August 1988 NS32532 data sheet.

1. The BF bit in the DCR register is not supported any longer and it should be set to 0.

2. The timing parameter tCASh is specified relative to the rising edge of BCLK instead of the falling edge.

The following are additional changes made since the October 1987 NS32532 data sheet which are included in the September 1988 data sheet.

1. If /BER is issued to the CPU during a burst transfer or a split bus cycle due to 8/16 bit bus, the CPU continues to bring in the remaining transactions. However, the CPU will ignore the remaining transactions and Bus Error routine will be entered correctly.

2. The branch prediction mechanism was modified so it predicts forward branches as taken for the instructions BLE and BNE.

3. Software must clear all bits in the DSR (RD included) when appropriate (Data Sheet Section 2.1.6).

4. When a debug condition is detected during execution of an instruction , the /BP signal is asserted at the beginning of the next instruction. If the instruction is aborted, /BP may or may not be asserted. (Data sheet section 3.3.2).

5. BCLK and /BCLK should see a capacitive load of at least 50 pf. The CPU requires this in order to meet the timing values specified in the data sheet. (section 4.4.2.1).

6. The custom slave instructions CATST0 and CATST1 are not supported. (Data sheet page 23).

7. /SDONE and /FSSR should be pulled high with 10k resistors.

8. Floating-point instructions are not interruptible. Therefore, the PSR I-flag is not transferred to the FPU. (Data sheet section 3.1.4.1).

9. If /BER is asserted during the ICU read cycle of a RETI instruction the HALT state is entered. (data sheet section 3.2.6).

10. A burst transfer or a regular multicycle transfer is not stopped by the assertion of /BER. However, the data read after the assertion of /BER is ignored.

11. CIOUT, /IOINH and U/S are not floated during HOLD acknowledge. Therefore, the timing parameters tUSf, tUSnf, tCOf, tCOnf, tIOIf and tIOInf should be eliminated.

12. The BF bit is removed from the DCR.

USER INFORMATION

NS32201 TCU Revision C

November 4, 1986

1. Under heavy current loads, the switching transients may cause the low level voltages on the output signals to reach levels slightly higher than those specified in the data sheet. This problem can be avoided by reducing the load on the output signals and using 'ROGERS' type capacitors as bypassing caps.

DATA SHEET CHANGES/CLARIFICATIONS
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1. If the CWAIT signal is generated asynchronously, it's set up and hold times may be violated. In this case it is recommended to synchronize it with CTTL to minimize the possibility of metastable states. The TCU provides only one synchronization stage in order to sample CWAIT as late as possible to avoid penalizing cases where CWAIT is generated synchronously.

2. As of revision G of the NS32032 or revision S of the NS32016, it is no longer required to provide a better Voh on the TCU PHI1, PHI2 outputs via 25 pf capacitors. Therefore, it is recommended that these capacitors be removed.

USER INFORMATION

NS32c201 TCU Revision B

November 30, 1987

1. Under heavy current loads, the switching transients may cause the low level voltages on the output signals to reach levels higher than those specified in the data sheet. This problem can be avoided by reducing the load on the output signals and using 'ROGERS' type capacitors as bypassing caps. Note that the part is specified to sink 2 mA when Vol is at 0.10Vcc (MAX for Vol). This is not the same as the NS32201 which is specified to sink 20 mA when Vol is at 0.5 volts.

2. The output signals of this revision of the NS32c201 may exhibit overshoot/ undershoot when switching from one state to another. The magnitude of the spikes depend on several conditions such as loading of the TCU outputs, placing of the TCU relative to the rest of the cluster, robustness of the TCU Vcc and GND inputs decoupling and the inductance of the TCU socket and the PC board traces. Therefore, it is recommended that zero ohm resistors be inserted on the PHIi paths to provide the capabality for slowing these signals in case the overshoot/ undershoot make the PHIi levels out of the CPU spec.

3. XIN input can withstand 1200 volts if tested for ESD using a human model.

USER INFORMATION

NS32C201 TCU Revision C

November 14, 1988

1. Under heavy current loads, the switching transients may cause the low level voltages on the output signals to reach levels higher than those specified in the data sheet. This problem can be avoided by reducing the load on the output signals and using 'ROGERS' type capacitors as bypassing caps. Note that the part is specified to sink 2 mA when Vol is at 0.10Vcc (MAX for Vol). This is not the same as the NS32201 which is specified to sink 20 mA when Vol is at 0.5 volts.

DATA SHEET CHANGES/CLARIFICATIONS

The following changes are related to the NS32C201 data sheet included in the 1988 data book.

1. The temperature range of the present parts is 0 to 70" C instead of -40 to 85" C.

2. The minimum Voh for PHI1 and PHI2 is 4.25 volts when the parts is operating at 4.5 volts (10% tolerance part).

3. The RC time constant shown in figures 1-3a and 1-3b should be long enough to ensure that /RSTI will be held low for at least 50 us after Vcc has reached 4.5 volts and at least 64 CTTL cycles have occured.

SUGGESTIONS

1. The output signals of the NS32c201 may exhibit overshoot/ undershoot when switching from one state to another due to the short rise and fall times. The magnitude of the spikes depends on the characteristics of the signal traces in the PC board as well as the loading of the signals. Therefore, it is recommended that the TCU be placed right next to the CPU and MMU (to minimize the effect of the traces), and zero ohm resistors be inserted on the PHI1 and PHI2 signal paths to provide the capability for adding damping resistors in case the overshoot/ undershoot become high enough to excede the maximum levels allowed by the CPU and MMU.

USER INFORMATION

NS32202-6 ICU, Revision E
NS32202-8 ICU, Revision E
NS32202-10 ICU, Revision E

July 24, 1985

1. It has been found that the upper NIBBLE of Reg. 1 (SVCT), gets spuriously transferred to Reg. 16 (MCTL). In particular, the bits which are SET (1's) in the upper NIBBLE of Reg. 1 set the corresponding bits in Reg. 16 to 1. This creates some undesirable effects in a NS32202 based system. The following suggestion should be considered to circumvent or to alleviate the problem.

   a. SOFTWARE METHOD

   Program the Bias Field 'BBBB' in Reg. 1 (SVCT) to 0001 Binary. This, at the most, may result in spuriously setting CLKM bit in Reg. 16 (MCTL). If the G0/IR0 ---- G3/IR6 lines are used from the ICU then they will output PULSED FORM instead of SQUARE WAVE FORM, programmed as counter output.

   Of course, the dispatch table and its corresponding entries should be changed accordingly. If this method is unacceptable then consider the following.

   b. HARDWARE METHOD

   An external 'OR' gate can be used to generate Address A4 to the ICU. The inputs of the gate are CS/ and either A4 or A5 from the CPU.

   DATA SHEET CHANGES/CLARIFICATIONS
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1. If edge-triggered interrupts are to be handled, the TPL register should be programmed before the ELTG register, contrary to what the initialization flowchart in the ICU data sheet implies. This prevents spurious interrupt requests from being generated during the ICU initialization from edge-triggered interrupt positions.

2. If any cascaded ICU is used, the CSRC register should be cleared during initialization (if the initialization does not follow a hardware reset) by writing zeroes into it. This should be done before setting the bits corresponding to the cascaded interrupt positions. This operation ensures that the 4-bit in-service counters (associated with each interrupt position to keep track of cascaded interrupts) always gets cleared when the ICU is re-initialized.

3. If the ICU initialization does not follow a hardware reset, the ISRV register should be cleared during initialization by writing zeroes into it.

4. If an external interrupt must be masked off, the CPU can do so by setting the corresponding bit in the IMSK register. However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it may have sampled the INT line before it is removed by the ICU. This causes the ICU to output a vector value of 'XF' Hex. To avoid this problem the above operation should be performed with the CPU INTERRUPTS DISABLED.

USER INFORMATION

NS32202-6 ICU, Revision F
NS32202-8 ICU, Revision F
NS32202-10 ICU, Revision F

July 24, 1985

DATA SHEET CHANGES/CLARIFICATIONS
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1. If edge-triggered interrupts are to be handled, the TPL register should be programmed before the ELTG register, contrary to what the initialization flowchart in the ICU data sheet implies. This prevents spurious interrupt requests from being generated during the ICU initialization from edge-triggered interrupt positions.

2. If any cascaded ICU is used, the CSRC register should be cleared during initialization (if the initialization does not follow a hardware reset) by writing zeroes into it. This should be done before setting the bits corresponding to the cascaded interrupt positions. This operation ensures that the 4-bit in-service counters (associated with each interrupt position to keep track of cascaded interrupts) always gets cleared when the ICU is re-initialized.

3. If the ICU initialization does not follow a hardware reset, the ISRV register should be cleared during initialization by writing zeroes into it.

4. If an external interrupt must be masked off, the CPU can do so by setting the corresponding bit in the IMSK register. However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it may have sampled the INT line before it is removed by the ICU. This causes the ICU to output a vector value of 'XF' Hex. To avoid this problem the above operation should be performed with the CPU INTERRUPTS DISABLED.

NATIONAL SEMICONDUCTOR SYSTEMS & APPLICATIONS GROUP

USER INFORMATION

NS32202 ICU Revision G

January 12, 1987

ITEM #1

Title: OUTPUT G7

DESCRIPTION:
When General Purpose pin G7 (IC pin4) is programmed as an output, Vol is 0.4 Volt at 0.8 mA.

SUGGESTED WORKAROUND AND COMMENTS:
When G7 is used as an output, the connected device(s) Low Level Input Current should not exceed -0.8mA .

AFFECTED REVISIONS: G1, before date-code 8708

FIXED IN REVISION: G2, after date-code 8708

DATA SHEET CHANGES/CLARIFICATIONS

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1. If edge-triggered interrupts are to be handled, the TPL register should be programmed before the ELTG register, contrary to what the initialization flowchart in the ICU data sheet implies. This prevents spurious interrupt requests from being generated during the ICU initialization from edge-triggered interrupt positions.

2. If any cascaded ICU is used, the CSRC register should be cleared during initialization (if the initialization does not follow a hardware reset) by writing zeroes into it. This should be done before setting the bits corresponding to the cascaded interrupt positions. This operation ensures that the 4-bit in-service counters (associated with each interrupt position to keep track of cascaded interrupts) always gets cleared when the ICU is re-initialized.

3. If the ICU initialization does not follow a hardware reset, the ISRV register should be cleared during initialization by writing zeroes into it.

4. If an external interrupt must be masked off, the CPU can do so by setting the corresponding bit in the IMSK register. However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it may have sampled the INT line before it is removed by the ICU. This causes the ICU to output a vector value of 'XF' Hex. To avoid this problem the above operation should be performed with the CPU INTERRUPTS DISABLED.

USER INFORMATION

NS32203 DMAC, Revision C

June 6, 1986

KNOWN PROBLEMS

1) No interrupt is issued and no TC status bit update performed on transfer complete, when search is specified and the DMA transfer is terminated by a match/no match condition before the length register (LNGT) reaches zero.

2) The entire status register gets cleared even if only one byte is read. This can be a problem when the DMAC is used with a 32008 CPU.

3) The NS32203 may ignore RDY/ if this is generated by the NS32201 due to a timing incompatibility. The problem can be solved by deleting the rising edge of RDY/ by at least a half clock cycle.

4) When a memory-to-memory transfer is performed and the REQ/ signal is activated by the IO device, the DMAC can terminate the operation without clearing the IO request. When the channel is enabled for another operation (indirect memory-to-memory or IO-to-memory), a transfer is initiated without the REQ/ signal being activated.

   The previously latched request can be cleared by performing a short (dummy) direct transfer (in auto transfer) between IO device and memory. This should not have side effects if the IO device is wired for indirect transfers only.

5) The DMAC does not respond to REQn when the DMAC CS/ signal is activated . This can be a problem when the DMAC CS/ signal is activated during the CPU executes a WAIT instruction . This problem can be bypassed by ensuring that the CS/ signal is inactive while the CPU is waiting.

6) In some parts the internal registers are not writeable at 10 MHz.

7) If burst mode and direct data transfer mode are both selected, the DMAC will not stop transfering data following the deactivation of REQn/.

POTENTIAL PROBLEMS AT 10 MHZ

8) Burst direct (not locked) - An idle state is inserted between memory transfers.

9) Burst indirect - The HOLD/ signal is released after one transfer.

10) The address bits A16 - A23 may be erroneus. This problem is most likely to occur when the device gets hot.

DATA SHEET CLARIFICATIONS

1) If an 8 bit transfer is specified, address bit A0 will determine the byte of the data-bus where the transfer takes place. If address A0 = 0 the transfer occurs on the low order byte. If A0 = 1 it occurs on the high order byte.

2) The address of the software vector register SVCT is 5C .

3) If a transfer block has an odd number of bytes or is not word aligned an 8 bit width for source and destination should be selected.

4) 16 bit IO transfers are not specified with 8 bit memory transfers.

5) Memory to memory transfers should have the same width.

6) When an 8-bit transfer is related to an IO device, the other half of the 16-bit data bus is considered as DON'T CARE, and the HBE/ signal may be activated.

7) The TC bits of the status register are set whenever a channel completes the operation, regardless of whether a match/no match condition occurred.

8) If single transfer mode is specified, the request signal from the IO device is edge-triggered. This means that the request signal must be temporarily deasserted between transfer cycles, otherwise only one transfer cycle will be performed. This can be accomplished by disabling REQn when ACKn is activated.

9) If an interrupt is enabled, the corresponding bit in the status register is not cleared (upon read) if the interrupt is not acknowledged.

10) Requests from other channels are not acknowledged in the middle of a word assembly/disassembly. If this is a problem, 8 bit transfers should be specified for both source and destination.

11) If an indirect transfer is selected, the data transfer can be halted by clearing the command code bits in the Command register (low-byte). This, however, should not be done during direct transfers. In this case a data transfer can be halted by writing zero into the Length register

12) The DMAC behaviour during burst mode, as described in the problem section above, will only be changed for "direct transfers". For indirect transfers, the NS32203 Rev. E will behave like previous revisions.

13) The remote configuration is not supported in the present revisions of the DMAC. Therefore we recommend you do not use the device in remote configuration until further notice.

USER INFORMATION

NS32203 DMAC, Revision D

May 20, 1986

KNOWN PROBLEMS

1) In burst transfer mode, memory to I/O, the DMAC continues making data transfers after REQn goes inactive.

DATA SHEET CLARIFICATIONS

1) If an 8 bit transfer is specified, address bit A0 will determine the byte of the data-bus where the transfer takes place. If address A0 = 0 the transfer occurs on the low order byte. If A0 = 1 it occurs on the high order byte.

2) The address of the software vector register SVCT is 5C .

3) If a transfer block has an odd number of bytes or is not word aligned an 8 bit width for source and destination should be selected.

4) 16 bit IO transfers are not specified with 8 bit memory transfers.

5) Memory to memory transfers should have the same width.

6) When an 8-bit transfer is related to an IO device, the other half of the 16-bit data bus is considered as DON'T CARE, and the HBE/ signal may be activated.

7) The TC bits of the status register are set whenever a channel completes the operation, regardless of whether a match/no match condition occurred.

8) If single transfer mode is specified, the request signal from the IO device is edge-triggered. This means that the request signal must be temporarily deasserted between transfer cycles, otherwise only one transfer cycle will be performed. This can be accomplished by disabling REQn when

ACKn is activated.

9) If an interrupt is enabled, the corresponding bit in the status register is not cleared (upon read) if the interrupt is not acknowledged.

10) Requests from other channels are not acknowledged in the middle of a word assembly/disassembly. If this is a problem, 8 bit transfers should be specified for both source and

11) Disabling a DMA transfer by writing into the command register (low), may cause the LNGT register as well as the SRC and DST registers to be spuriously changed. The problem occurs when 'direct mode' and 'single transfers' are selected. No spurious transfer is performed when this happens.

USER INFORMATION

NS32203 DMAC, Revision F

March 12, 1987

DATA SHEET CLARIFICATIONS

1) If an 8 bit transfer is specified, address bit A0 will determine the byte of the data-bus where the transfer takes place. If address A0 = 0 the transfer occurs on the low order byte. If A0 = 1 it occurs on the high order byte.

2) If a transfer block has an odd number of bytes or is not word aligned an 8 bit width for source and destination should be selected.

3) 16 bit IO transfers are not specified with 8 bit memory transfers.

4) Memory to memory transfers should have the same width.

5) The TC bits of the status register are set whenever a channel completes the operation, regardless of whether a match/no match condition occurred.

6) If an interrupt is enabled, the corresponding bit in the status register is not cleared (upon read) if the interrupt is not acknowledged.

USER INFORMATION

NS32081-6 FPU, Revision D
NS32081-8 FPU, Revision D
NS32081-10 FPU, Revision D

November 13, 1985

1. The MOVLF instruction, with Operand 1 value of zero, will return the correct value of zero, but will set the Underflow Flag bit in the FSR. If the UEN (Underflow Trap Enable) bit is set, a TRAP(FPU) will occur. This will be corrected in the Rev. E NS32081.

2. While transferring operands into the Rev. D FPU, do not allow any delays between SPC pulses longer than 10 milliseconds. Doing so will cause this revision of the FPU to lose its internal state until the next FPU instruction is initiated. One observed side-effect of this has been a string of SPC pulses coming from the FPU, which may falsely activate other slave processors. In NS32000-based systems, do not allow DMA bursts longer than 10 milliseconds during FPU instructions, and if an abort occurs during an FPU instruction make certain that the abort trap handler promptly executes an FPU instruction in order to cancel the protocol that was in progress. This problem will be corrected in the Rev. E NS32081.

3. Performing a conversion from floating-point to integer (instructions: ROUND, TRUNC or FLOOR) on certain odd integral values (examples: 1.0, 3.0) and all negative integral values generates an erroneous inexact result flag. This will be corrected in the Rev. E NS32081.

4. If the FPU is used in a system that includes the MMU and the MMU aborts the fetch of the last word of the final operand, when the instruction is retried following the abort service routine the FPU will not latch the new operand data. This will cause the result of the retried instruction to be incorrect. To workaround this bug, the SFSR instruction should be used in the abort routine before doing any other floating point instruction. This will be corrected in the Rev. F NS32081.

5. Any combination of instruction/operands which cause both an underflow condition and an inexact result condition may return the wrong result if the Floating Status Register

(FSR) is set such that the underflow trap is disabled, and the inexact result trap is enabled. To bypass this problem, avoid setting the FSR to the stated values.

DOCUMENTATION CLARIFICATION

The following are clarifications or corrections to the current NS32081 FPU documentation:

1. When the FPU signals that it is finished processing an instruction (by pulsing the SPC pin low), it is necessary to wait for at least two cycles of the clock (CLK) before reading the Status Word. Series 32000 CPU's satisfy this requirement.

2. After reading the Status Word from the FPU, it is necessary to wait for three cycles of the CLK clock before reading a result. Series 32000 CPU's satisfy this requirement.

3. Whenever an FPU error condition occurs, the FSR TT field is loaded with the error code, regardless of whether that condition is enabled to cause a trap. An FPU instruction can therefore complete normally and still display a code of 001 (Underflow) or 110 (Inexact Result). This code remains in the TT field only until the next floating-point instruction (other than SFSR) completes. Early documentation has strongly implied that the TT field will appear non-zero only if a trap actually occurs. This has been fixed in the Series 32000 Instruction Set Reference Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

4. The FSR TT field is loaded with a new error status value (zero if no error) at the end of every floating-point instruction except LFSR or SFSR. (The LFSR instruction loads the TT field, but with the value supplied by the programmer instead of with error status). Most documentation to date, however, has stated that the FSR TT field is altered only if an error occurs or if the LFSR instruction is executed. The necessary changes appear in the Series 32000 Instruction Set Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

5. Asynchronous timing of SPC pulses with respect to CLK does not work reliably. Transfers to the FPU must follow NS32000-series CPU timing exactly: i.e., the SPC pulse must start shortly after a CLK rising edge and terminate shortly after the next rising edge. If the FPU is used as a Slave

Processor with a Series 32000 CPU, it should be clocked with the TCU CTTL signal. The necessary changes have been made in the Series 32000 Databook.

6. When transferring the ID Byte and the Operation Word to the FPU, there must be a gap of at least one clock cycle between T4 of the ID Byte transfer and T1 of the Operation Word transfer. Failure to do this can make register-to-register forms of FPU instructions execute unreliably. This requirement is met by 32000-series CPU's. Data sheets and Application Note AN383 do not yet mention it.

7. The value given for the DC characteristic II (Input Leakage Current) is incorrect. It should be -20 uA (min) to +20 uA (max).

8. The parameter tDf is 50 ns maximum for all speed versions. The parameter tSPCFnf is 0 minimum for all versions.

9. The minimum clock frequency (CLK pin) is 4 Mhz instead of 200 Khz as stated in the data sheet.

10. When the FPU is used in a system that includes the MMU, the FPU RST pin must be tied to the system reset, not the RST/ABT pin of the MMU.

USER INFORMATION

NS32081-6 FPU, Revision E
NS32081-8 FPU, Revision E
NS32081-10 FPU, Revision E

November 13, 1985

1. If the FPU is used in a system that includes the MMU and the MMU aborts the fetch of the last word of the final operand, when the instruction is retried following the abort service routine the FPU will not latch the new operand data. This will cause the result of the retried instruction to be incorrect. To workaround this bug, the SFSR instruction should be used in the abort routine before doing any other floating point instruction. This will be corrected in the Rev. F NS32081.

2. Any combination of instruction/operands which cause both an underflow condition and an inexact result condition may return the wrong result if the Floating Status Register (FSR) is set such that the underflow trap is disabled, and the inexact result trap is enabled. To bypass this problem, avoid setting the FSR to the stated values.

DOCUMENTATION CLARIFICATION

The following are clarifications or corrections to the current NS32081 FPU documentation:

1. When the FPU signals that it is finished processing an instruction (by pulsing the SPC pin low), it is necessary to wait for at least two cycles of the clock (CLK) before reading the Status Word. Series 32000 CPU's satisfy this requirement.

2. After reading the Status Word from the FPU, it is necessary to wait for three cycles of the CLK clock before reading a result. Series 32000 CPU's satisfy this requirement.

3. Whenever an FPU error condition occurs, the FSR TT field is loaded with the error code, regardless of whether that condition is enabled to cause a trap. An FPU instruction can therefore complete normally and still display a code of

001 (Underflow) or 110 (Inexact Result). This code remains in the TT field only until the next floating-point instruction (other than SFSR) completes. Early documentation has strongly implied that the TT field will appear non-zero only if a trap actually occurs. This has been fixed in the Series 32000 Instruction Set Reference Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

4. The FSR TT field is loaded with a new error status value (zero if no error) at the end of every floating-point instruction except LFSR or SFSR. (The LFSR instruction loads the TT field, but with the value supplied by the programmer instead of with error status). Most documentation to date, however, has stated that the FSR TT field is altered only if an error occurs or if the LFSR instruction is executed. The necessary changes appear in the Series 32000 Instruction Set Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

5. Asynchronous timing of SPC pulses with respect to CLK does not work reliably. Transfers to the FPU must follow NS32000-series CPU timing exactly: i.e., the SPC pulse must start shortly after a CLK rising edge and terminate shortly after the next rising edge. If the FPU is used as a Slave Processor with a Series 32000 CPU, it should be clocked with the TCU CTTL signal. The necessary changes have been made in the Series 32000 Databook.

6. When transferring the ID Byte and the Operation Word to the FPU, there must be a gap of at least one clock cycle between T4 of the ID Byte transfer and T1 of the Operation Word transfer. Failure to do this can make register-to-register forms of FPU instructions execute unreliably. This requirement is met by 32000-series CPU's. Data sheets and Application Note AN383 do not yet mention it.

7. The value given for the DC characteristic II (Input Leakage Current) is incorrect. It should be -20 uA (min) to +20 uA (max).

8. The parameter tDf is 50 ns maximum for all speed versions. The parameter tSPCFnf is 0 minimum for all versions.

9. The minimum clock frequency (CLK pin) is 4 Mhz instead of 200 Khz as stated in the data sheet.

10. When the FPU is used in a system that includes the MMU, the FPU RST pin must be tied to the system reset, not the RST/ABT pin of the MMU.

USER INFORMATION

NS32081 FPU, Revision F

June 2, 1987

1. Any combination of instruction/operands which cause both an underflow condition and an inexact result condition may return the wrong result if the Floating Status Register (FSR) is set such that the underflow trap is disabled, and the inexact result trap is enabled. To bypass this problem, avoid setting the FSR to the stated values.

DOCUMENTATION CLARIFICATION

The following are clarifications or corrections to the current NS32081 FPU documentation:

1. When the FPU signals that it is finished processing an instruction (by pulsing the SPC pin low), it is necessary to wait for at least two cycles of the clock (CLK) before reading the Status Word. Series 32000 CPU's satisfy this requirement.

2. After reading the Status Word from the FPU, it is necessary to wait for three cycles of the CLK clock before reading a result. Series 32000 CPU's satisfy this requirement.

3. Whenever an FPU error condition occurs, the FSR TT field is loaded with the error code, regardless of whether that condition is enabled to cause a trap. An FPU instruction can therefore complete normally and still display a code of 001 (Underflow) or 110 (Inexact Result). This code remains in the TT field only until the next floating-point instruction (other than SFSR) completes. Early documentation has strongly implied that the TT field will appear non-zero only if a trap actually occurs. This has been fixed in the Series 32000 Instruction Set Reference Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

4. The FSR TT field is loaded with a new error status value (zero if no error) at the end of every floating-point instruction except LFSR or SFSR. (The LFSR instruction loads the TT field, but with the value supplied by the programmer instead of with error status). Most documentation to date, however, has stated that the FSR TT field is altered only if an error occurs or if the LFSR instruction is executed. The necessary changes appear in the Series 32000 Instruction Set Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

5. Asynchronous timing of SPC pulses with respect to CLK does not work reliably. Transfers to the FPU must follow NS32000-series CPU timing exactly: i.e., the SPC pulse must start shortly after a CLK rising edge and terminate shortly after the next rising edge. If the FPU is used as a Slave Processor with a Series 32000 CPU, it should be clocked with the TCU CTTL signal. The necessary changes have been made in the Series 32000 Databook.

6. When transferring the ID Byte and the Operation Word to the FPU, there must be a gap of at least one clock cycle between T4 of the ID Byte transfer and T1 of the Operation Word transfer. Failure to do this can make register-to-register forms of FPU instructions execute unreliably. This requirement is met by 32000-series CPU's. Data sheets and Application Note AN383 do not yet mention it.

7. The value given for the DC characteristic II (Input Leakage Current) is incorrect. It should be -20 uA (min) to +20 uA (max).

8. The parameter tDf is 50 ns maximum for all speed versions. The parameter tSPCFnf is 0 minimum for all versions.

9. The minimum clock frequency (CLK pin) is 4 Mhz for NS32081-10 and 8 Mhz for NS32081-15 instead of 200 Khz as stated in the data sheet.

10. When the FPU is used in a system that includes the MMU, the FPU RST pin must be tied to the system reset, not the RST/ABT pin of the MMU.

USER INFORMATION

NS32081 FPU, Revision H

August 23, 1988

DOCUMENTATION CLARIFICATION

The following are clarifications or corrections to the current NS32081 FPU documentation:

1. When the FPU signals that it is finished processing an instruction (by pulsing the SPC pin low), it is necessary to wait for at least two cycles of the clock (CLK) before reading the Status Word. Series 32000 CPU's satisfy this requirement.

2. After reading the Status Word from the FPU, it is necessary to wait for three cycles of the CLK clock before reading a result. Series 32000 CPU's satisfy this requirement.

3. Whenever an FPU error condition occurs, the FSR TT field is loaded with the error code, regardless of whether that condition is enabled to cause a trap. An FPU instruction can therefore complete normally and still display a code of 001 (Underflow) or 110 (Inexact Result). This code remains in the TT field only until the next floating-point instruction (other than SFSR) completes. Early documentation has strongly implied that the TT field will appear non-zero only if a trap actually occurs. This has been fixed in the Series 32000 Instruction Set Reference Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

4. The FSR TT field is loaded with a new error status value (zero if no error) at the end of every floating-point instruction except LFSR or SFSR. (The LFSR instruction loads the TT field, but with the value supplied by the programmer instead of with error status). Most documentation to date, however, has stated that the FSR TT field is altered only if an error occurs or if the LFSR instruction is executed. The necessary changes appear in the Series 32000 Instruction Set Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

5. Asynchronous timing of SPC pulses with respect to CLK does not work reliably. Transfers to the FPU must follow NS32000-series CPU timing exactly: i.e., the SPC pulse must start shortly after a CLK rising edge and terminate shortly after the next rising edge. If the FPU is used as a Slave Processor with a Series 32000 CPU, it should be clocked with the TCU CTTL signal. The necessary changes have been made in the Series 32000 Databook.

6. When transferring the ID Byte and the Operation Word to the FPU, there must be a gap of at least one clock cycle between T4 of the ID Byte transfer and T1 of the Operation Word transfer. Failure to do this can make register-to-register forms of FPU instructions execute unreliably. This requirement is met by 32000-series CPU's. Data sheets and Application Note AN383 do not yet mention it.

7. The minimum clock frequency (CLK pin) is 4 Mhz instead of 200 Khz as stated in the data sheet.

8. When the FPU is used in a system that includes the MMU, the FPU RST pin must be tied to the system reset, not the RST/ABT pin of the MMU.

9. The Typical Icc is now specified as 200 ma.

10. The minimum tDf is now specified as 2ns for 15 MHz parts.

ERRATA SHEET
NS32381 FPU Revision B
October 31, 1988

1. The instructions DIVf , DIVl may produce wrong results. To workaround this problem, emulate the DIVf, DIVl instructions by software. (B-1,2,3,4).

2. The MOVif instruction may produce wrong results when preceded by DIVf or DIVl. Workaround : same as 1. (B-1).

3. The SCALB instruction will hang the system if the absolute value of opr1 is less than 1 and if the absolute value of opr2 is equal to zero. It will hang for both the SCALBF and SCALBL instructions. Workaround : Check opr2 for each SCALB instruction and test for opr2 = +/- 0.0 and if true, return opr2 as the result. (B2-1).

4. The DOT and POLY instructions can miss an Inexact Result condition if the exponent of the "ADD" is within one of the exponent of the product term and the operands have opposite signs. (C-2).

   Example:
   ```
   srcf0:  double h'407ff000
   src1 :  double h'3ef81e00
   src2 :  double h'bfe00000

       LFSR 0              ; Clear Inexact Flag (IF)
       MOVF srcf0, f0      ; Initialize f0
       POLYF src1, src2    ; The product term has more sig-
                           ; nificant bits than the NS32381
                           ; has internally and thus bits are
                           ; lost in forming the Inexact Result.
   ```

   In the above example the FSR's IF bit will not be set and if the IEN bit is set the Inexact Result Trap will not occur and the TT field is unaffected.

   * This Inexact Result bug using the DOT and POLY instructions is a data dependent bug and will not occur in most cases.

DATA SHEET CHANGES / CLARIFICATIONS

The following changes should be made to the October 1987 NS32381 data sheet.

1. The following pins are CMOS inputs and should never float: NOE, PS0 and PS1.
   NOTE: Ground or pull-up with 1K ohm resistors as per the application.

2. The following RESERVED pins should be tied to ground:
   A10, B1 and B9.

3. The following RESERVED pins should be left floating:
   B8, F1, K7 and K10.

4. The minimum Input Load Current for NOE, PS0 and PS1 is -100 uA and the maximum is 100 uA.

5. The minimum Icc will not be specified.

6. The Data Invalid for the 32-Bit Slave Protocol NS32532 CPU parameter, tDiv, has been changed and is now referenced to "After CLK R.E." instead of "After SPC/ T.E." and the minimum is 3 ns instead of 18 ns at both 15 and 20 MHz.

7. The Slave Done Active for the 32-Bit Slave Protocol NS32532 CPU parameter, tSDa, has been changed and the maximum is 40 ns at 15 Mhz and the maximum is 35 ns at 20 MHz.

8. The Forced Slave Status Read Active for the 32-Bit Slave Protocol NS32532 CPU parameter, tFSSRa, has been changed and the maximum is 40 ns at 15 MHz and the maximum is 35 ns at 20 MHz.

9. Two new parameters have been added to the NS32381 "Input Signal Requirments for the 32-Bit Slave Protocol NS32532 CPU".

Symbol	Figure	Description	Reference/Conditions	381-15 MIN	381-15 MAX	381-20 MIN	381-20 MAX	
tSPCia	4-14	SPC/Inactive	After CLK(T1)R.E.	0		0		ns
tSPCa	4-14	SPC/Active	After CLK(T1)R.E.	3		3		ns

10. In the Power Down Mode the NS32381 will consume only 10% of its original power at 30 Mhz and the maximum power down current for Iout=0, TA=25 degree C is 30 mA at 30 MHz.

ERRATA SHEET
NS32381 FPU Revision B2
October 31, 1988

1. The SCALB instruction will hang the system if the absolute value of opr1 is less than 1 and if the absolute value of opr2 is equal to zero. It will hang for both the SCALBF and SCALBL instructions. Workaround : Check operand 1 and skip the SCALB instruction if the absolute value of operand 1 is less than 1.0. (B2-1).

   * The SCALB instruction contains a data dependent bug but will function properly in most cases.

2. The POLY instruction will erroneously indicate the underflow condition if one of the product terms is zero and the magnitude of the other is less than 1.0 or equal to zero. (B2-2).

```
Example: movf  0.5, f0    ;initialize f0
         polyf 0.0, 12.34 ;(0.0*0.5)+12.34 =12.34 exactly => f0
                          ;but this instruction will set the
                          ;underflow flag and trap if the UEN
                          ;bit is set.
```

   If the UEN bit is not set then f0 will contain the correct result but the FSR will have the wrong value.

   * The POLY instruction also contains a data dependent bug and will also function properly in most cases.

3. The DOT and POLY instructions can miss an Inexact Result condition if the exponent of he "ADD" is within one of the exponent of the product term and the operands have opposite signs. (C-2).

```
Example:
srcf0:  double h'407ff000
src1 :  double h'3ef81e00
src2 :  double h'bfe00000


    LFSR 0              ; Clear Inexact Flag (IF)
    MOVF srcf0, f0      ; Initialize f0
    POLYF src1, src2    ; The product term has more sig-
                        ; nificant bits than the NS32381
                        ; has internally and thus bits are
                        ; lost in forming the Inexact Result.
```

   In the above example the FSR's IF bit will not be set and if the IEN bit is set the Inexact Result Trap will not occur and the TT field is unaffected.

* This Inexact Result bug using the DOT and POLY instructions is a data dependent bug and will not occur in most cases.

DATA SHEET CHANGES / CLARIFICATIONS

The following changes should be made to the June 1988 NS32381 data sheet and the Series 32000 Microprocessor Databook, Rev. 1.

1. The title should include "/NS32381-25/NS32381-30" speed versions of the part.

2. Delete the DDIN/ signal from Figures 3-4b and 3-4c.

3. Section 4.4.2.1 should read: Output Signal Propagation Delays for all CPUs (16-Bit Slave Protocol).

4. Delete the "1/2" for all values of tSPCFw in section 4.4.2.1.

5. The max. tSPCFa is 17ns for both 15 and 20MHz parts in section 4.4.2.1.

6. The symbol tSPCFi should read tSPCFia and the min. value of 18ns should be deleted from both the 15 and 20MHz specifications in section 4.4.2.1.

7. The symbol tSPCFnf should read tSPCFf and its description should read: "SPC/ Output Floating" in section 4.4.2.1.

8. In section 4.4.2.3 the following symbol and description changes should be made respectively:
   tDiv to tDh and "Data Invalid" to "Data Hold"
   tDnf to tDf and "Data Nonforcing" to "Data Floating"
   tSDNnf to tSDNf and "Slave Done Nonforcing" to "Slave Done Floating"

9. In section 4.4.2.4 tDv should read 93ns for 15mHz, 68ns for 20MHz, 54ns for 25MHz and 45ns for 30MHz for the max. Data Valid after SPC/ L.E.

10. In section 4.4.2.4 the following symbol and description changes should be made respectively:
    tDiv to tDh and "Data Invalid" to "Data Hold"
    tDnf to tDf and "Data Nonforcing" to "Data Floating"
    tSDnf to tSDf and "Slave Done Nonforcing" to " Slave Done Floating"
    tFSSRnf to tFSSRf and "Forced Slave Status Read Nonforcing" to "Forced Slave Status Read Floating"

11. In section 4.4.2.9 tCLKp should read 66.6ns for the min. clock period for 15MHz parts.

12. Remove the sentence, "The NS32381 FPU conforms to IEEE standard 754-1985 for binary floating-point arithmetic.", from the 2nd paragraph in the General Description.

13. Remove the 3rd statement from the Features list, "Conforms to IEEE standard 754-1985 for binary floating-point arithmetic".

14. Section 1.1 should read "IEEE FEATURES SUPPORTED - Standard 754-1985".

15. Remove from section 1.1 the entire paragraph , "The remaining IEEE features are supported in software. These items include ... ".

16. Delete the word "proposed" and "(Task P754)" from the 1st paragraph of section 1.2.3.

17. Delete the phrase "by means of its hardware and software features" from the 1st paragraph of section 1.0.

18. In Figure 3-4c the " RST/ " is missing from the NS32381's reset signal.

19. In Figures 3-4b and 3-4c the TCU should read " NS32C201 ".

20. In section 4.4.2.5 the description of tRSTs should read " Reset Setup Time ", the Reference/Conditions should read " Before CLK R.E. " and the minimum values need to be characterized for each frequency.

21. In Appendix A the EXT and EDD timing terms are measured in the number of clock cycles.

ERRATA SHEET
NS32381 FPU Revision C
October 26, 1988

1. The POLY instruction will hang the system if one or both of the product terms is zero.

   Example:

```
MOVF   0.5, f0      ; Initialize f0
POLYF  0.0, 12.34   ; (0.0 * 0.5) + 12.34
                    ; This instruction will HANG the system
                    ; since operand 1 equals zero.  (C-1).
```

   * This condition must be avoided if using the POLY instruction.

2. The DOT and POLY instructions can miss an Inexact Result condition if the exponent of the "ADD" is within one of the exponent of the product term and the operands have opposite signs. (C-2).

   Example:

```
srcf0:  double h'407ff000
src1 :  double h'3ef81e00
src2 :  double h'bfe00000


    LFSR    0             ; Clear Inexact Flag (IF)
    MOVF    srcf0, f0     ; Initialize f0
    POLYF   src1, src2    ; The product term has more sig-
                          ; nificant bits than the NS32381
                          ; has internally and thus bits are
                          ; lost in forming the Inexact Result.
```

   In the above example the FSR's IF bit will not be set and if the IEN bit is set the Inexact Result Trap will not occur and the TT field is unaffected.

   * This Inexact Result bug using the DOT and POLY instructions is a data dependent bug and will not occur in most cases.

   DATA SHEET CHANGES / CLARIFICATIONS

   The following changes should be made to the June 1988 NS32381 data sheet and the Series 32000 Microprocessor Databook, Rev. 1.

1. The title should include "/NS32381-25/NS32381-30" speed versions of the part.

2. Delete the DDIN/ signal from Figures 3-4b and 3-4c.

3. Section 4.4.2.1 should read: Output Signal Propagation Delays for all CPUs (16-Bit Slave Protocol).

4. Delete the "1/2" for all values of tSPCFw in section 4.4.2.1.

5. The max. tSPCFa is 17ns for both 15 and 20MHz parts in section 4.4.2.1.

6. The symbol tSPCFi should read tSPCFia and the min. value of 18ns should be deleted from both the 15 and 20MHz specifications in section 4.4.2.1.

7. The symbol tSPCFnf should read tSPCFf and its description should read: "SPC/ Output Floating" in section 4.4.2.1.

8. In section 4.4.2.3 the following symbol and description changes should be made respectively:
   tDiv to tDh and "Data Invalid" to "Data Hold"
   tDnf to tDf and "Data Nonforcing" to "Data Floating"
   tSDNnf to tSDNf and "Slave Done Nonforcing" to "Slave Done Floating"

9. In section 4.4.2.4 tDv should read 93ns for 15mHz, 68ns for 20MHz, 54ns for 25MHz and 45ns for 30MHz for the max. Data Valid after SPC/ L.E.

10. In section 4.4.2.4 the following symbol and description changes should be made respectively:
    tDiv to tDh and "Data Invalid" to "Data Hold"
    tDnf to tDf and "Data Nonforcing" to "Data Floating"
    tSDnf to tSDf and "Slave Done Nonforcing" to " Slave Done Floating"
    tFSSRnf to tFSSRf and "Forced Slave Status Read Nonforcing" to "Forced Slave Status Read Floating"

11. In section 4.4.2.9 tCLKp should read 66.6ns for the min. clock period for 15MHz parts.

12. Remove the sentence, "The NS32381 FPU conforms to IEEE standard 754-1985 for binary floating-point arithmetic.", from the 2nd paragraph in the General Description.

13. Remove the 3rd statement from the Features list, "Conforms to IEEE standard 754-1985 for binary floating-point arithmetic".

14. Section 1.1 should read "IEEE FEATURES SUPPORTED - Standard 754-1985".

15. Remove from section 1.1 the entire paragraph , "The remaining IEEE features are supported in software. These items include ... ".

16. Delete the word "proposed" and "(Task P754)" from the 1st paragraph of section 1.2.3.

17. Delete the phrase "by means of its hardware and software features" from the 1st paragraph of section 1.0.

18. In Figure 3-4c the " RST/ " is missing from the NS32381's reset signal.

19. In Figures 3-4b and 3-4c the TCU should read " NS32C201 ".

20. In section 4.4.2.5 the description of tRSTs should read " Reset Setup Time ", the Reference/Conditions should read " Before CLK R.E. " and the minimum values need to be characterized for each frequency.

21. In Appendix A the EXT and EDD timing terms are measured in the number of clock cycles.

ERRATA SHEET
NS32580 FPC Revision A
June 27, 1988

1. In the PIPE MODE the FSR contains the wrong value if the first instruction in the pipe is SQRTf or DIVf and there are four other instructions in the pipe with the fifth instruction being LFSR. (177).
   NOTE: When counting instructions, count the following instructions a two instructions: MACF/L, MOViF (only float), CMPF/L, NEGF/L and MOVL Mem, Reg. (even registers only)

2. In the PIPE MODE the NS32580 will dead lock if the first instruction in the pipe is SQRTf or DIVf, the forth instruction in the pipe is CMPf and the operands of the CMPf cause a Trap in SUBf. See note above. (178).

3. In the PIPE MODE one of the Floating-Point registers gets the wrong value if the (i) instruction in the pipe is NEGf and the (i-1) or (i-2) instruction causes a trap, where i is the number of the instruction in the pipe. (183).

4. In the PIPE MODE the result of SFSR can be wrong if the first instruction in the pipe is SQRTf or DIVf and there are four other instructions in the pipe with the fifth instruction being SFSR. See note in 1. (186).

5. In the PIPE MODE with 3-Cycle Latency enabled the FSR can have the wrong value if the (i) instruction in the pipe is MULL and the (i+1) instruction in the pipe is MOViF. (187).

   NOTE: MOViF : i= B/W/D, F- only single precision

6. In the PIPE MODE the NS32580 will dead lock if the n, n+1 instructions in the pipe return traps and the n+2 or n+3 instruction in the pipe returns a trap. See note in 1. (188).

   NOTE: The following double instructions can cause two traps:
   MACf => MULf and ADDf
   CMPf => SUBf and CMPf

USER INFORMATION

NS32082 MMU, Rev. L

November 12, 1985

1. Breakpoints can not be used reliably with this revision of MMU.

2. Since the MMU alters the state of the M bit position in the Level-1 Page Table Entry (PTE), due to a bug in this revision of MMU, Level-1 PTE's should be initialized with the M bit position set to avoid any inefficiency. To workaround another bug in the current revision, the M bit in the Level-2 PTE should always be kept set.

3. Upon powering up the MMU and placing it in 16-bit mode (A24 pin held high on the rising edge of RST, see Data Sheet Clarification item "b" below), the MMU may be placed in a mode in which it actively asserts an address (contents undefined) on the A16-A24 pins through T1 of the first memory cycle performed by the CPU. This address conflicts with the address asserted by the CPU during T1 (which should be zero), causing the first word of the first instruction to be fetched from an incorrect address. In 32-bit mode, the incorrect initialization has no side effects, and the MMU recovers without symptoms. 32-bit mode can be used in 32016-based systems if address bits A16-A24 are latched in the same manner as AD0-AD15.

4. HOLD should not be asserted during MMU slave instructions and during MMU initiated bus cycles (FLT active).

Data Sheet Clarifications

The following are clarifications or corrections to the March 1982 NS32082 Data Sheet:

a. The Program Flow features and Non-Sequential Trace Trap are being deleted as features of the MMU. The registers PF0, PF1 and SC are no longer supported. The MSR bits FT, UT and NT should always be kept zero for future compatibility.

b. There is a new 32-bit bus mode strap option not documented in the current data sheet. Pin A24 is sampled at reset. If A24 is high, 16-bit bus mode is selected, and the MMU operates as documented. If A24 is low, 32-bit bus mode is selected for use with the NS32032 microprocessor. In 32-bit bus mode, the MMU drives addresses on lines AD0-AD23 only during TMMU and during Page Table lookups, freeing these bus pins for data transfer from T2-T4. All address bits, including A16-A23, must be latched on PAV in this mode.

c. The BST, EST, BD, ED, TET and ERC fields are cleared if and only if the MSR is loaded with a value in which bit 1 is set (e.g.: hex 00010002 enables User Mode translation and clears the above status fields).

d. As of MMU Revision G, it is no longer true that the BPR0 register cannot count write cycles. Bits BW and CE may both be set (DBG16 options /W and /C both selected).

   As of MMU Revision H, however, there remains a limitation that the BR, BW and CE bits must not all be set (DBG16 options /R,/W and /C).

e. The MMU alters the state of bit 4 of Level-1 Page Table Entries. Any information stored in that bit by software will be destroyed.

1. Physical breakpoints can not be used reliably.

2. HOLD should not be asserted during MMU slave instructions and during MMU initiated bus cycles (FLT active).

3. If the SMR instruction is aborted, the NS32082 will not get reset upon execution of any non-MMU slave instruction in the abort routine. To bypass this bug the first slave instruction in the abort routine should be an MMU instruction.

Data Sheet Clarifications

The following are clarifications or corrections to the March 1982 NS32082 Data Sheet:

a. The Program Flow features and Non-Sequential Trace Trap are being deleted as features of the MMU. The registers PF0, PF1 and SC are no longer supported. The MSR bits FT, UT and NT should always be kept zero for future compatibility.

b. There is a new 32-bit bus mode strap option not documented in the current data sheet. Pin A24 is sampled at reset. If A24 is high, 16-bit bus mode is selected, and the MMU operates as documented. If A24 is low, 32-bit bus mode is selected for use with the NS32032 microprocessor. In 32-bit bus mode, the MMU drives addresses on lines AD0-AD23 only during TMMU and during Page Table lookups, freeing these bus pins for data transfer from T2-T4. All address bits, including A16-A23, must be latched on PAV in this mode.

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As of MMU Revision H, however, there remains a limitation that the BR, BW and CE bits must not all be set (DBG16 options /R,/W and /C).

e. The MMU alters the state of bit 4 of Level-1 Page Table Entries. Any information stored in that bit by software will be destroyed.

f. The minimum clock frequency for the NS32082 is 4 MHz instead of 200 kHz as stated in the data sheet. At this frequency the maximum clock high voltage (on PHI1, PHI2) pins is Vcc instead of Vcc + 0.5 Volt.

g. The minimum time for tDDINf (figure 4-7 in the 1986 SERIES 32000 databook) may be a value less than zero. This, however, does not cause any conflict with the timing requirements of TCU and CPU for the DDIN signal .

USER INFORMATION

NS32082 MMU, Rev. N

April 25, 1986

1. If the NS32332 is running a four clock cycle bus with the NS32082, then a revision N of the NS32082 should be used. In this case the U/S output pin of the NS32082 should be synchronized to PHI2 clock.

2. If the SMR instruction is aborted, the NS32082 will not get reset upon execution of any non-MMU slave instruction in the abort routine. To bypass this bug the first slave instruction in the abort routine should be an MMU instruction.

Data Sheet Clarifications

The following are clarifications or corrections to the March 1982 NS32082 Data Sheet:

a. The Program Flow features and Non-Sequential Trace Trap are being deleted as features of the MMU. The registers PF0, PF1 and SC are no longer supported. The MSR bits FT, UT and NT should always be kept zero for future compatibility.

b. There is a new 32-bit bus mode strap option not documented in the current data sheet. Pin A24 is sampled at reset. If A24 is high, 16-bit bus mode is selected, and the MMU operates as documented. If A24 is low, 32-bit bus mode is selected for use with the NS32032 microprocessor. In 32-bit bus mode, the MMU drives addresses on lines AD0-AD23 only during TMMU and during Page Table lookups, freeing these bus pins for data transfer from T2-T4. All address bits, including A16-A23, must be latched on PAV in this mode.

c. The BST, EST, BD, ED, TET and ERC fields are cleared if and only if the MSR is loaded with a value in which bit 1 is set (e.g.: hex 00010002 enables User Mode translation and clears the above status fields).

d. As of MMU Revision G, it is no longer true that the BPR0 register cannot count write cycles. Bits BW and CE may both be set (DBG16 options /W and /C both selected).

As of MMU Revision H, however, there remains a limitation that the BR, BW and CE bits must not all be set (DBG16 options /R,/W and /C).

e. The MMU alters the state of bit 4 of Level-1 Page Table Entries. Any information stored in that bit by software will be destroyed.

f. The minimum clock frequency for the NS32082 is 4 MHz instead of 200 kHz as stated in the data sheet. At this frequency the maximum clock high voltage (on PHI1, PHI2) pins is Vcc instead of Vcc + 0.5 Volt.