4.0 Device Specifications (Continued)

4.1 NS32SF641 PIN DESCRIPTIONS

Table 4-1 lists the signals in alphabetical order. A description of the packaging and electrical characteristics of the NS32SF641 follows.

TABLE 4-1. Table of Interface Signals

Symbol	Pins	Signal Name	I/O	Active	TRI-STATE®
A0–31	32	Address Bus	I/O		Yes
ADS0	1	Address Strobe 0	Output	High	No
ADS1	1	Address Strobe 1	Output	High	No
$\overline{BE0-7}$	8	Byte Enable (0–7)	Output	Low	Yes
$\overline{BP}$	1	Break Point	Output	Low	No
$\overline{BRT}$	1	Bus Retry	Input	Low	
BW0–1	2	Bus Width (0–1)	Input	Encode	
CASEC/ BW64	1	Cache Section/ 64-Bit Default Bus (Sampled at Reset)	I/O	Encode Encode	Yes
$\overline{CBE}$	1	Configuration Buffer Enable	Output	Low	No
CIIN	1	Cache Inhibit In	Input	High	
CIOUT	1	Cache Inhibit Out	Output	High	
CLK	1	Bus Clock	Input		
D0–63	64	Data Bus (0–63)	I/O		Yes
$\overline{DAK0}$	1	DMA Acknowledge 0	Output	Low	No
$\overline{DAK1}$	1	DMA Acknowledge 1	Output	Low	No
DCLK	1	Delayed Bus Clock	Output		No
$\overline{DDIN}$/ $\overline{TST}$	1	Data Direction In/ Self Test Enable (Sampled at Reset)	I/O	Low Low	Yes
$\overline{DRD}$	1	Data Read	Output	Low	Yes
$\overline{DRQ0}$	1	DMA Request 0	Input	Low	
$\overline{DRQ1}$	1	DMA Request 1	Input	Low	
DSEL	1	Data Select	Output	Encode	Yes
$\overline{DWR0}$	1	Data Write Strobe 0	Output	Low	Yes
$\overline{DWR1}$	1	Data Write Strobe 1	Output	Low	Yes
$\overline{EOT}$	1	End Of DMA Transfer	Input	Low	
$\overline{ERR}$	1	Error	Output	Low	No
$\overline{HLDA}$	1	Hold Acknowledge	Output	Low	No
$\overline{HOLD}$	1	Hold Request	Input	Low	
$\overline{IDLE}$	1	Idle Cycle Request	Input	Low	

Note 1: All of the output signals of the NS32SF641, except for $\overline{ERR}$, are TRI-STATE while in Shadow mode. The TRI-STATE column of Table 4-1 refers only to the state of the signal during hold, extended-retry, and reset.

Symbol	Pi
$\overline{ILO}$	
$\overline{INVBLK}$	
$\overline{INVDC}$	
$\overline{INVIC}$	
$\overline{IR0-3}$	4
$\overline{IREF}$	
ISE	
$\overline{NMI}$	1
$\overline{PAGE}$	1
$\overline{PFSA}$	1
$\overline{PFSB}$	1
PIPEN	1
$\overline{PLAT}$	1
PT2	1
$\overline{RDY}$	1
$\overline{RST}$	1
SCLK	1
SDIO	1
$\overline{SDDIN}$	1
$\overline{SHDW}$	1
ST0–3	4
$\overline{STALL}$	1
TXA	1
TXB	1
$\overline{TRIS}$	1
U/$\overline{S}$/ $\overline{ILVD}$	1
WAIT	1
$\overline{XBRTA}$	1

Note 1: All of the output signa
state of the signal during hol
Note 2: During reset SDIO is