istics of the NS32SF641

TRI-STATE®
Yes
No
No
Yes
No
Yes
No
Yes
No
No
No
Yes
Yes
Yes
Yes
Yes
No
No

f Table 4-1 refers only to the

4.0 Device Specifications (Continued)

TABLE 4-1. Table of Interface Signals (Continued)

Symbol	Pins	Signal Name	I/O	Active	TRI-STATE®
$\overline{ILO}$	1	Interlocked Bus Cycle	Output	Low	No
$\overline{INVBLK}$	1	Invalidate Block	Input	Low	
$\overline{INVDC}$	1	Invalidate Data Cache	Input	Low	
$\overline{INVIC}$	1	Invalidate Instruction Cache	Input	Low	
$\overline{IR}0-3$	4	Maskable Interrupt (0–3)	Input	Encode	
$\overline{IREF}$	1	Internal Reference	Output	Low	No
ISE	1	In-System Emulation (Sampled at Reset)	Input	High	
$\overline{NMI}$	1	Non-Maskable Interrupt	Input	Edge	
$\overline{PAGE}$	1	Same Page	Output	Low	Yes
$\overline{PFSA}$	1	Program Flow Status (Pipe-A)	Output	Low	No
$\overline{PFSB}$	1	Program Flow Status (Pipe-B)	Output	Low	No
PIPEN	1	Pipelined Bus Enable	Input	High	
$\overline{PLAT}$	1	Page Latch Enable	Input	Low	
PT2	1	Possibe T2 of the Bus Cycle	Output	High	Yes
$\overline{RDY}$	1	Ready	Input	Low	
$\overline{RST}$	1	Reset	Input	Low	
SCLK	1	Serial Link Clock	Input	Edge	
SDIO	1	Serial Data I/O	I/O		No
$\overline{SDDIN}$	1	Serial Link Data Direction In	Output	Low	No
$\overline{SHDW}$	1	Shadow Mode	Input	Low	
ST0–3	4	Status (0–3)	Output	Encode	No
$\overline{STALL}$	1	Stall	Input	Low	
TXA	1	Timer Control	I/O	High	No
TXB	1	Timer Trigger	Input	High	
$\overline{TRIS}$	1	TRI-STATE All Outputs	Input	Low	
U/$\overline{S}$/ $\overline{ILVD}$	1	User/Supervisor Mode/ Interleaved Memory (Sampled at Reset)	I/O	Encode Encode	Yes
WAIT	1	Wait	Input	High	
$\overline{XBRTA}$	1	Extended Bus Retry Acknowledge	Output	Low	No

Note 1: All of the output signals of the NS32SF641, except for $\overline{ERR}$, are TRI-STATE while in Shadow mode. The TRI-STATE column of Table 4-1 refers only to the state of the signal during hold, extended-retry, and reset.

Note 2: During reset SDIO is also in TRI-STATE.