VNS-N16

VNS-N16 VME - Central Processing Unit with NS32000

Specifications:

* NS 32016 CPU

* Demand Paged Virtual Memory Management

* High speed Floating Point-
  Instructions (32bit and 64bit)

* Up to 256kByte battery-buffered CMOS-RAM

* Up to 256kByte EPROM

* VMEbus-Interface (VME Spec. Rev. B)

* Tri Port Memory

* Dual-Port

* CMOS real time clock

The VMEbus-Board "VNS-N16" carries the complete NS 32000 mikroprocessor chip set, as there are:

NS 32016	CPU	Central Processing Unit
NS 32082	MMU	Memory Managment Unit
NS 32201	TCU	Timing / Control Unit
NS 32081	FPU	Floating Point Unit
NS 32202	ICU	Interrupt Control Unit

This Central Unit includes a 32-Bit microprocessor, a Floating Point Unit (with 32-Bit and 64-Bit) and a virtual Memory Management Unit.
This VMEbus compatible unit has especially been developed for applications, where large data quantities have to be processed. It is in detail used for CAD/CAM-Systems, industrial control equipments, image processing, integrated office-systems, army electronics and tele-communications and particularly where 16-Bit computers aren't sufficient.

MEMORY

There are 128k-Byte battery-buffered CMOS-RAM on board of the "VNS-N16". This memory can be expanded to its double capacity of 256k-Byte CMOS RAM.
This memory is transparent for external accesses, e. g. DMA-Controllers or Co-Processors, that means that DMA-Controllers can access memory from both busses without disturbing the efficiency of the NS32016.

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This way it is possible to do "page-swapping" or to build up spool-files by the aid of slave-processors during normal program running time.
With a free definable USER ADDRESS-MODIFIER the NS32016 processor can be stopped from the bus 2 (P2). In this case the CPU outputs are tri-state, so that a very fast data transfer (> 6MByte/sec) can be performed.
Furtheron for user programs and monitor program two EPROM sockets for capacities from 64k-Bit up to 512k-Bit are available. An expansion up to 256k-Byte PROM is also possible.

INTERFACE

Two interrupt driven serial channels represent the interfaces to the peripheral world. One of it is for the system terminal and the other for computer coupling features. Channel B is user definable RS232 or up to 800k-Baud RS422 (HDLC/SDLC, BISYNC).

REAL TIME CLOCK

The battery-buffered real-time-clock with time, date and year is able to generate interrupts within 0,01sec up to 1 year intervals; applications are protocolling and alert messages.

BUS-INTERFACE

The "VNS-N16" has two bus-interfaces available:

connector P1 = standard VMEbus
connector P2 = row a and c free configurable

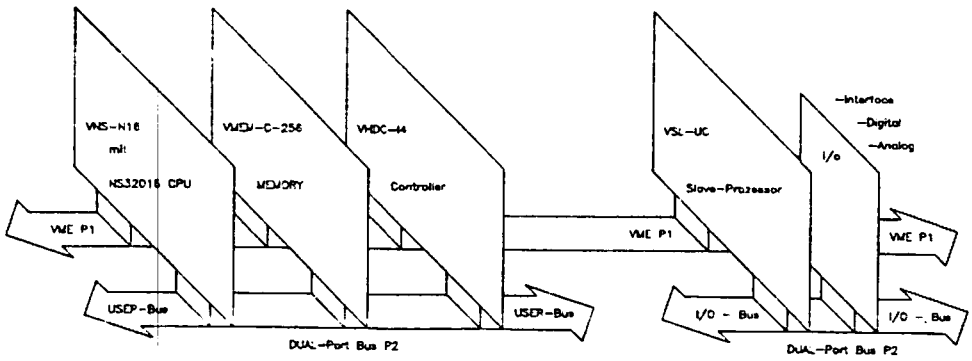
The second bus using connector P2 places approximatly the same signals and the same timing as the VMEbus at the user's disposal. The main difference is, that the signal-lines aren't directly connected to the plug P2 but can be free programmed by using a wrapp-field. Additionally by the help of a PAL® of his own choice the user is able to generate other signals or change the timing. With this option mainly all 8Bit- or 16Bit busses can be adapted to connector P2 (e.g. ECB, EURO, G64, Z-BUS, PMB a.s.o.). This makes a further usage of existent 8Bit or 16Bit CPU-, I/O- or memory-boards as well possible as an adaption to other plug-systems like S100 or Multi-Bus.
An on-board synchronisation logic supervises the access of both busses and of the CPU to the on-board memory. Because of the used logic a so called DEAD-LOCK is in any case out of question.

DUAL-PORT-PRINCIPLE

The very special conception of this central unit using two busses and a TRI-PORT-Memory considerably increases system throughput. Slave-processors for disk-operation, DMA, graphics and peripheral devices are able to work simultaniously without disturbing system activities and unburdon the CPU from pure data-transfer or management jobs.

VNS-N16

DUAL - PORT Prinzip



Both busses are able to manage DMA or Interrupts. A Status Register pins the CPU down wether it shall access external memory or peripheric via bus A or bus B. This feature prevents the CPU from waiting for a free bus if DUAL-PORT-Memory-boards like "MEM-C-256" or slave-processors like "VSL-UC" are used. If none of the busses is occupied by a bus-master, bus choice is free.
With a DMA or a second CPU the on-board memory can be accessed directly.
By the connector P2 it is possible to carry out very fast data transfers. Therefore, however, timing must be modified.
This modification is allowed, because it is done within the USER-I/O lines a1-a32 and c1-c32 at P2.
In this mode and with a modified timing transfer-rates of about 8M-Bytes/sec can be reached.

BUFFERING

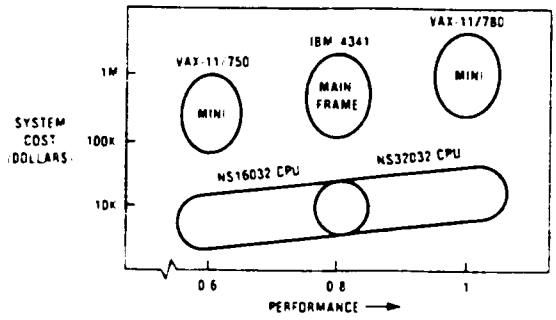
In case of power-supply breakdowns RAM and the CMOS-Clock are switched off after the necessary power-fail-procedures (stand-by). The on-board rechargeable battery then take over the supplying of the RAMs and the clock for min. 2500h (100 days).

VIRTUAL MEMORY MANAGEMENT

In most computer systems the CPU addressable memory block is larger than the physically available memory. Therefore the programmer is forced to fit his programs to the existent memory; this generates an additional software overhead.
The formidable advantage of the here used "demand paging" over "segmentation", in general, is the simplicity with witch pages can be swapped in and out of main memory. The result is a particularly low-overhead memory allocation algorithm that improves system performance.
The programmer may utilize the hole logic address space without taking care of memory management, even if the physical memory isn't large enough.

VNS-N16

The simplicity and efficiency of the "Demand-Paged" virtual memory management realized by the NS32000-family have former only been features of much larger systems. The development of the "VNS-N16" including all features of the NS32000-family makes the efficiency of Minis available to the user for the expense of Micros.



Comparison NS32000 / Minis and Mainframes

SOFTWARE

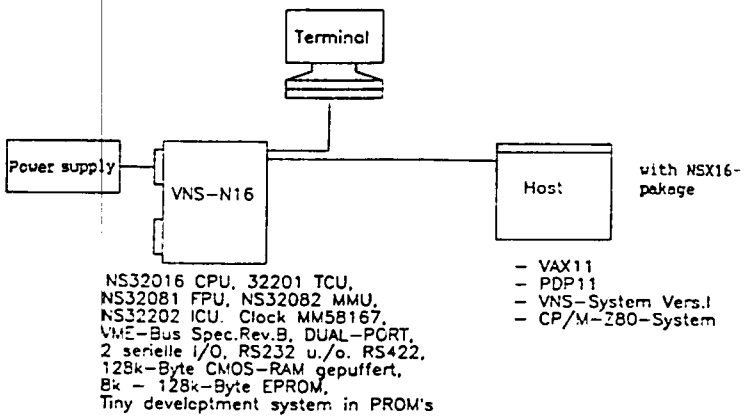
A debugger-monitor for developing and testing is delivered with the board. Furtheron existent systems (e. g. VAX, PDP11, CP/M, SYS32, VNS-SYS) can be used for software development in future with the help of the cross-software pakage "NSX16".
This "NSX16"-pakage includes:
Pascal-Compiler, NS32000 Cross-Assembler, Cross-Linker a.o.

Further Program-Languages: FORTRAN 77, C-Compiler, ADA, BASIC, FORTH, a.m.m.

Operating Systems: UNIX, GENIX, UNIX SYSTEM V, XENIX, a.o.

Likewise a REAL-TIME-Kernel "RTM" for real Multi-User-, Multi-Tasking-, Real-Time-Processing is available.

VNS-N16 VME-Board with NS32000-family



VNS-N16 as development board (transparent mode)

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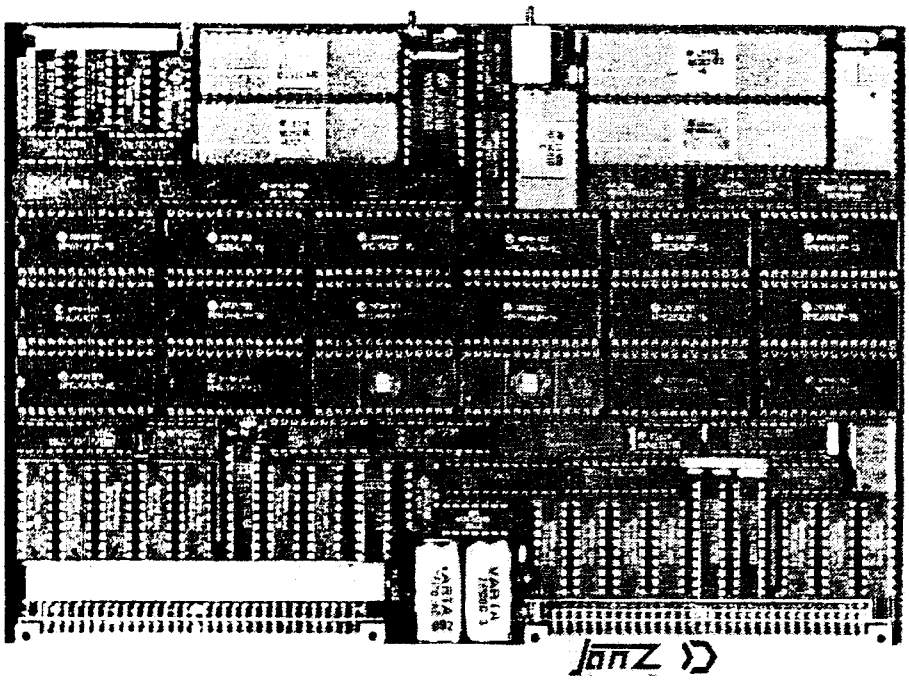
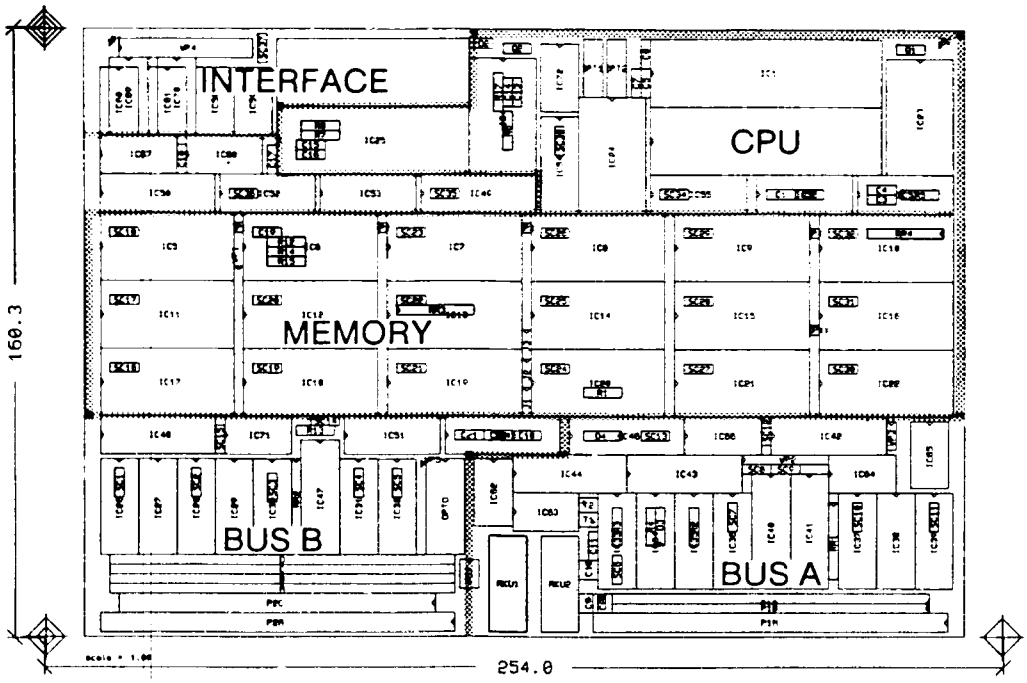
VNS-N16 VME - Central Processing Unit with NS32000





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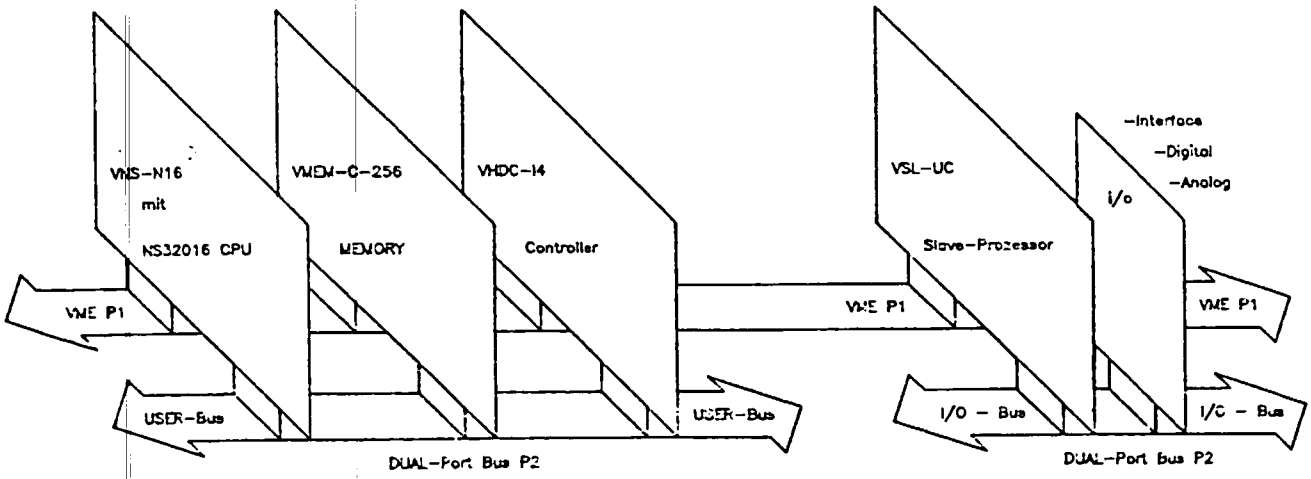
DUAL – PORT Prinzip

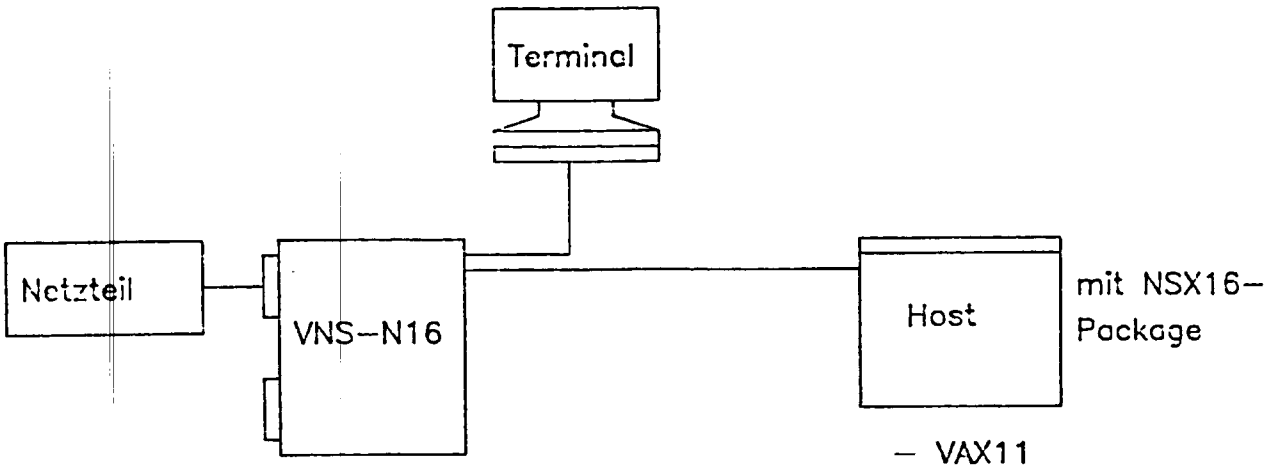
VME und ein flexibles 2.Bussystem



Bus P1 nach VME Spec.Rev.B

Bus P2 (VG-Leiste a + c) frei waehlbar
- -Signalbelegung und Timing konfigurierbar
- -Adaption an 8Bit- und 16Bit-Bussysteme
- -voll DMA- und interruptfaehig

VNS-N16 VME-Board mit NS32000-Familie



mit NS32016 CPU, 32201 TCU,
NS32081 FPU, NS32082 MMU,
NS32202 ICU. Clock MM58167,
VME-Bus Spec.Rev.B, DUAL-PORT,
2 serielle I/O, RS232 u./o. RS422,
128k-Byte CMOS-RAM gepuffert,
8k – 128k-Byte EPROM,
Tiny developtment system in FROM's

- VAX11
- PDP11
- VNS-System Vers.I
- CP/M-Z80-System

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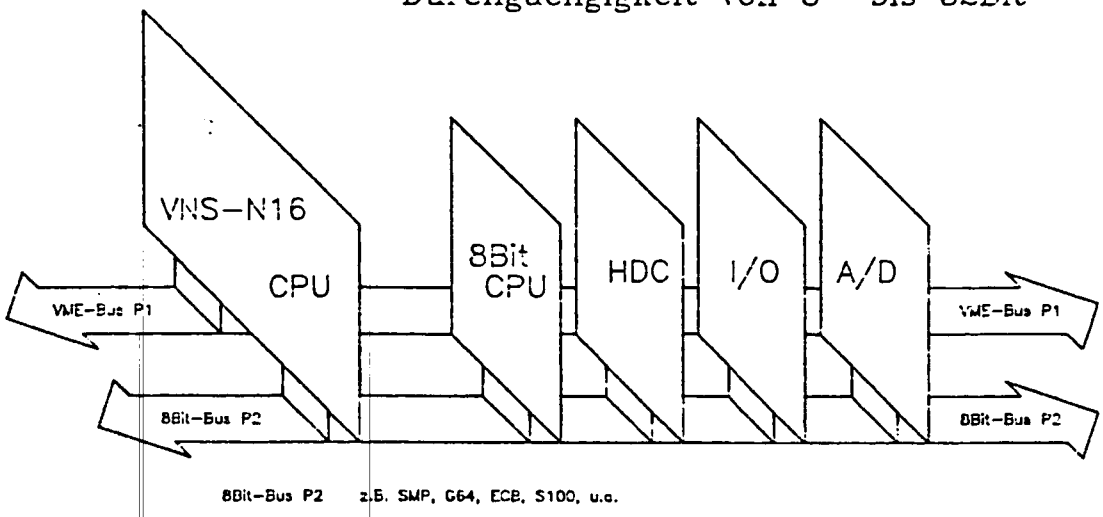
VME-Bus mit DUAL-PORT

-- Anpassung von 8Bit-Systemen
-- P2 konfigurierbar ueber PAL und Wrapp
-- Durchgaengigkeit von 6- bis 32Bit



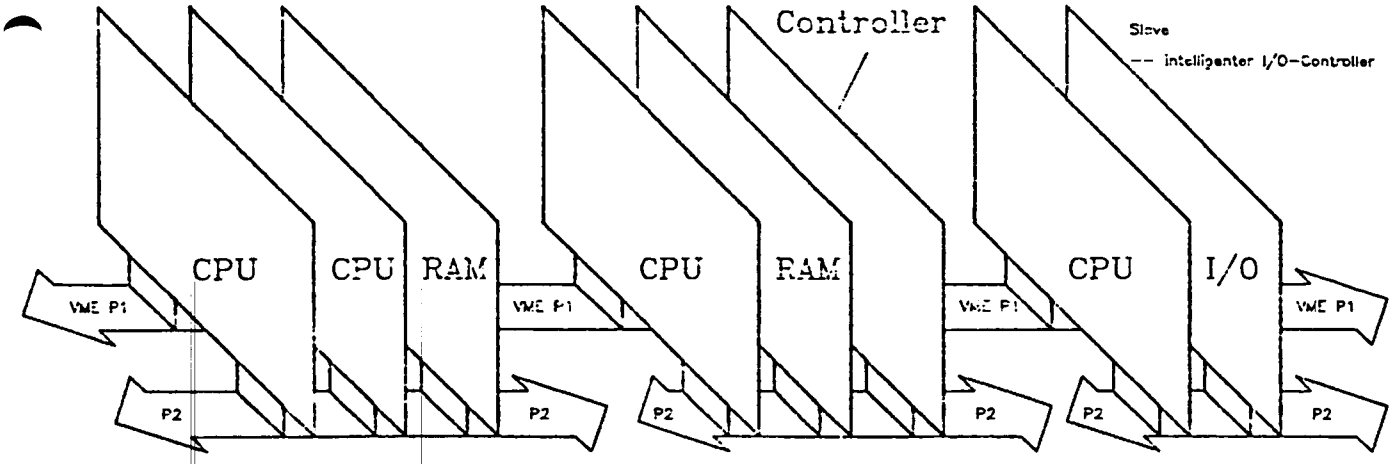
8Bit-Bus P2 z.B. SMP, G64, ECB, S100, u.a.

Multiprozessor-System

Anwendung des DUAL-PORT-Prinzips

2 Busse, ein allgemeiner Bus (VME, P1), ein frei definierbarer Bus (P2)

-- Erhoehung der Performance
mehrere Prozessoren koennen simultan arbeiten



Multiprozessor-System verbunden ueber VME-Bus (P1)

P2 kann fuer jeden Block konfiguriert werden

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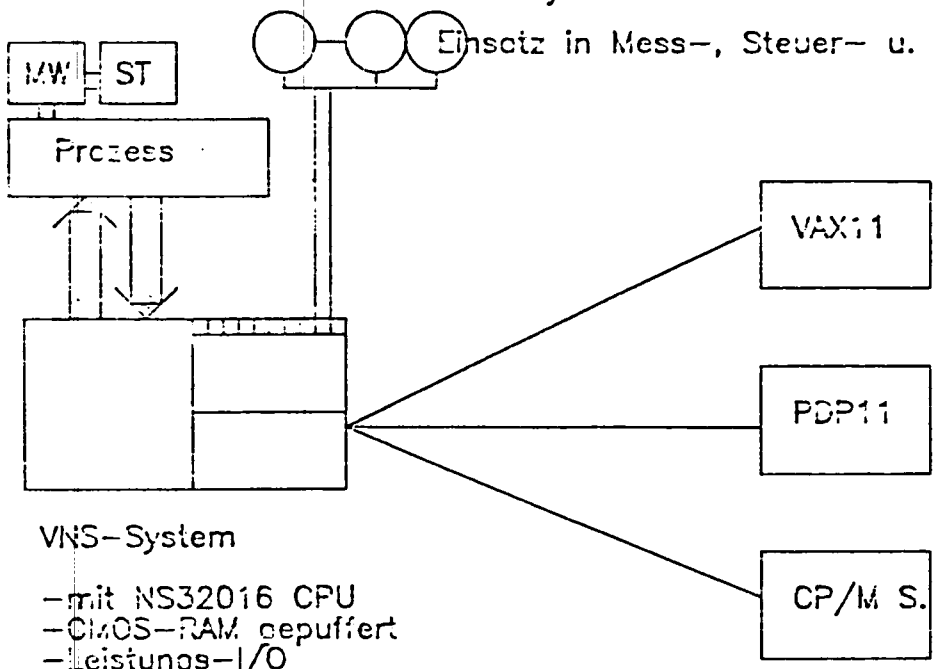
VME - System mit NS32000

Einsatz in Mess-, Steuer- u. Regeltechnik



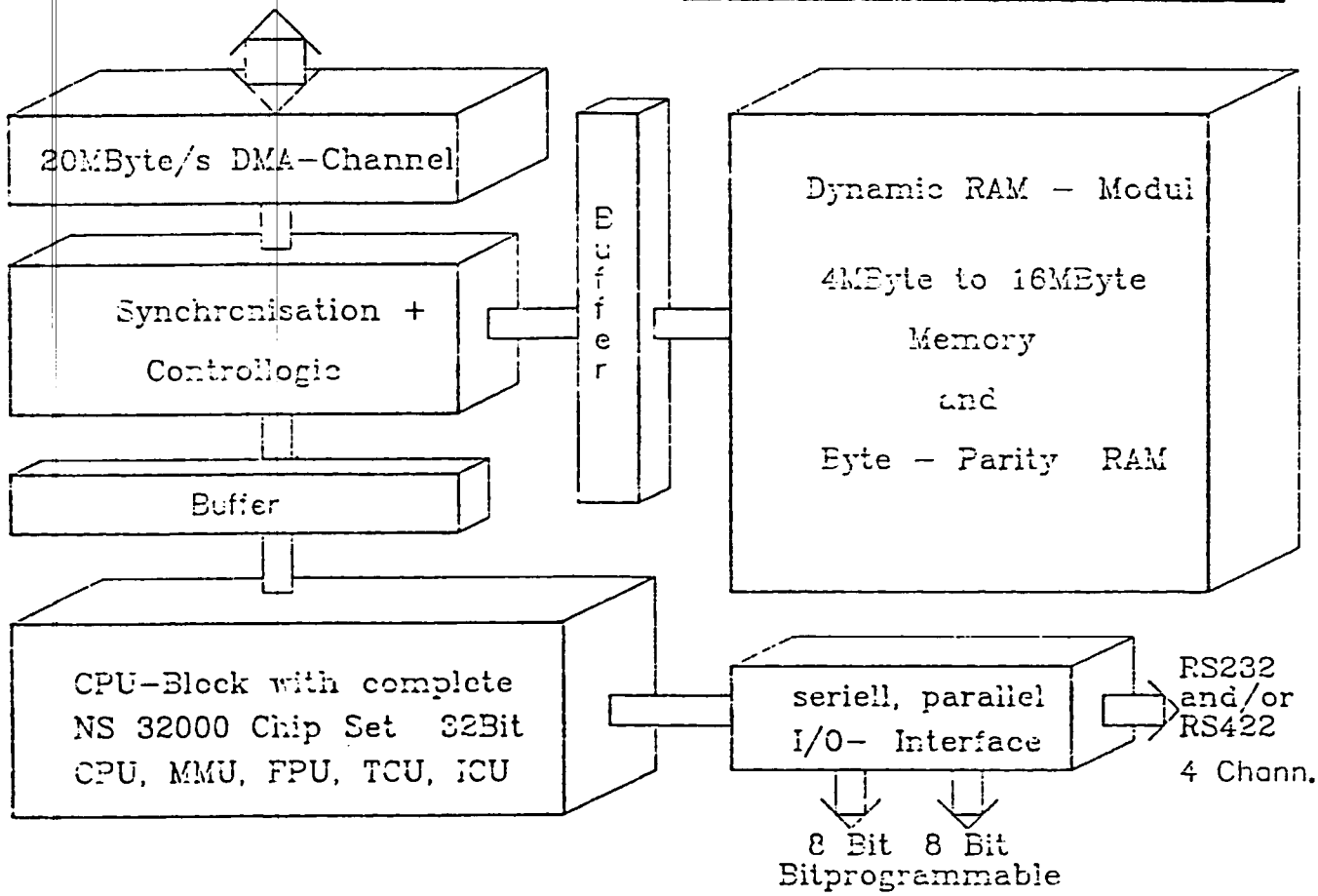
Host-Systeme

-Programmentwicklung und zentrale BDE

VNS-System

- mit NS32016 CPU
- CMOS-RAM gepuffert
- Leistungs-I/O
- Real-Time-Kernel (RTM)
- Erweiterung mit VME-Moduln
  z.B. Digital-Regler,
  PDV-Interface,
  A/D- u. D/A-Moduln.

Blockdiagram MAXI32000



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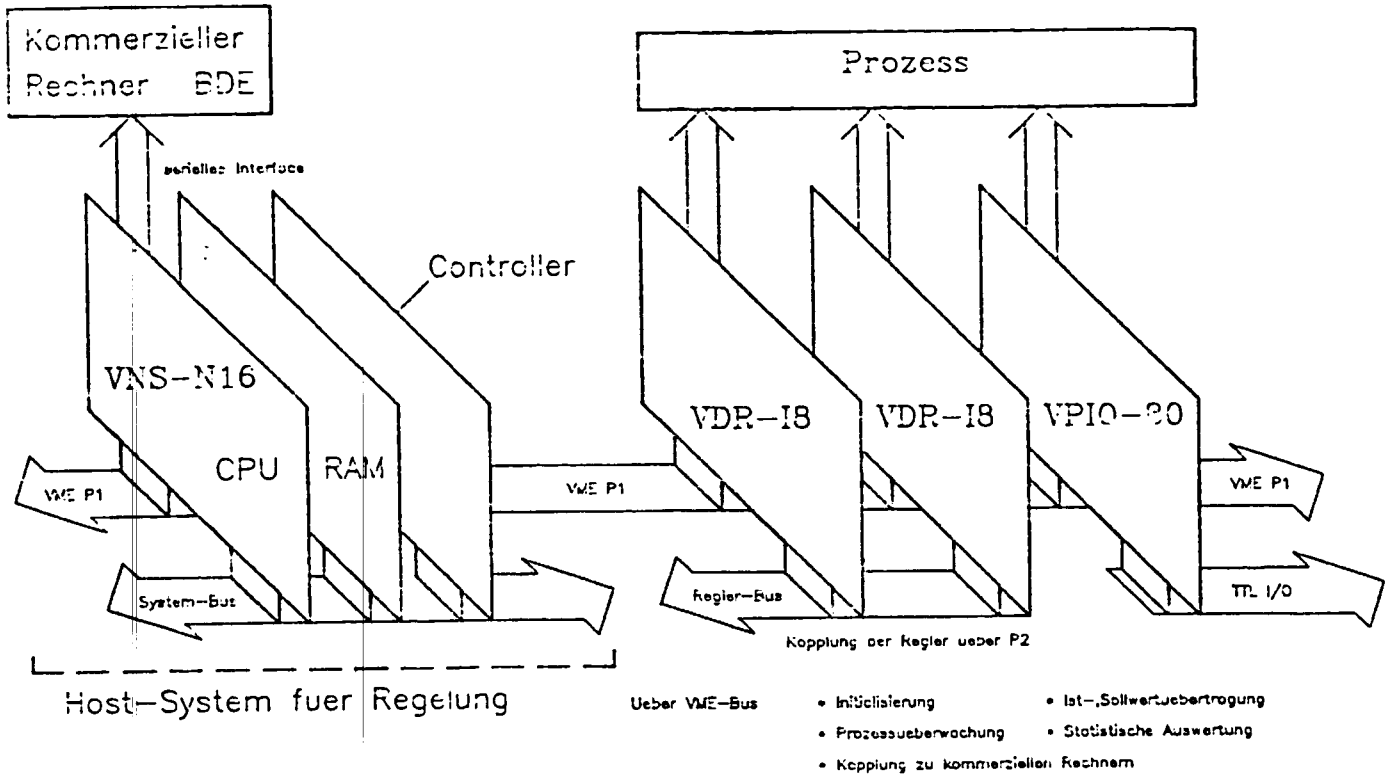
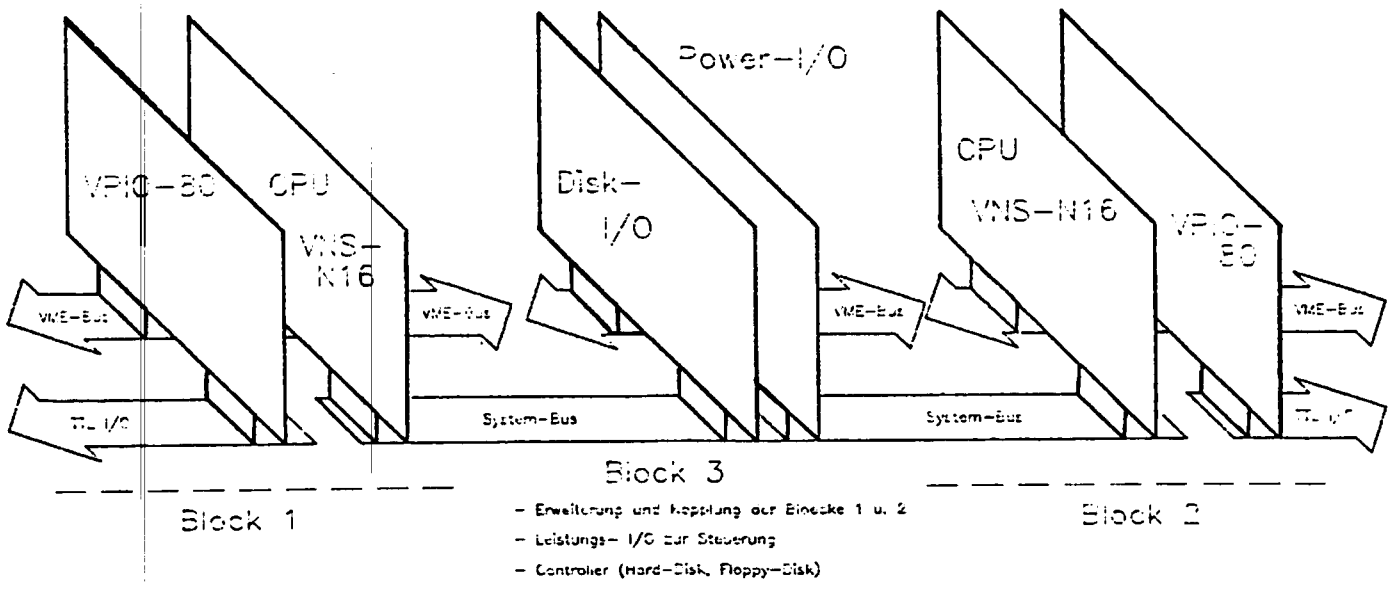
Regler-Konzept mit VDR-I8



Messdatenerfassung und -verarbeitung, Steuerung

Messwerterfassung (digital) mit VPIO-80, -verarbeitung und Steuerung mit VNS-N16



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VEPR-256 EPROM/RAM - MODUL

* 256kByte RAM and/or EPROM

* Battery buffered

* Dual port, P1 = VME-bus
  P2 = free configurable bus

* User definable interface on P2

* VMEbus compatible Rev.B

The VEPR-256 is a RAM/EPROM board able to carry up to 32 JEDEC-standard memory circuits. It is a Dual-Port-Memory for computer systems based on the VMEbus.
The RAM or PROM selection can be done with jumpers. Usable RAM's and EPROM's are the 8k by 8bit memory family.

The connector P1 has a standard interface configurated for the VMEbus Rev B.
The P2 connector represents a complete bus interface, with all important VMEbus signals available. Only the rows a and c are used by this connector. The board signals are not wired directly to connector P2, but to a wrapp-field. The choice of pin connections on rows a and c can consist of any combination the user prefers.

Apart from this there is a socket for a 20pin IC next to the wrapp-field. Any 0.3" IC, especially PALs, can hereby be used to cover any requirements the user may have. So other timings and signals can be generated. This enables P2 to match itself to another 8bit bus e.g. ECB, EURO, G64 or to another 16bit bus e.g. Z-BUS, MULTIBUS.

P2 can be used by a harddisk- or another controller to free the systembus from CPU actions.

A special on board logic provides the management of both busses. Because of an READ-MODIFY-WRITE-Command a Semaphore-Management is possible. During an ASCENDING ACCESS memory is locked. This provides a secure File-Handling. Memory data access of both busses is not possible because of a logic on board decides in a less than 10ns time which Bus is to be preferred. A priority cannot be given.

Because of the on board NC accumulator, RAM data on the VEPR-256 isn't lost during power failure. This allows further data save procedures.

The VEPR-256 is switched off by SYS-Reset or by Vcc less than 4,5V.

The board can be appointed as an USER or SYSTEM memory by the selection of the Addressmodifier.
The VEPR-256 is able to work with the ASCENDING ACCES MODE on both busses. This allows the user to operate with highest transfer rates (more than 9M-Byte/s).

Total access time = memory access time plus 60ns

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VMEM-C-256 STATIC CMOS-RAM MODUL

* 256kyte static CMOS RAM

* Battery buffered

* Dual port, P1 = VME-bus
  P2 = free configurable bus

* User definable interface on P2

* VMEbus compatible Rev.B

The VMEM-C-256 consists 256kbyte static CMOS RAM. It is a Dual-Port-Memory for computer systems based on the VMEbus.

The connector P1 has a standard interface configurated for the VME Bus (Rev B).

The P2 connector represents a complete bus interface, with all important VMEbus signals available. Only the rows a and c are used by this connector. The board signals are not wired directly to connector P2, but to a wrapp-field. The choice of pin connections on rows a and c can consist of any combination the user prefers.

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Because of the on board NC accumulator, RAM data on the VMEM-C-256 isn't lost during power failure. This allows further data save procedures.

The VMEM-C-256 is switched off by SYS-Reset or by Vcc less than 4,5V.

The board can be appointed as an USER or SYSTEM memory by the selection of the Addressmodifier.
The VMEM-C-256 is able to work with the ASCENDING ACCES MODE on both busses. This allows the user to operate with highest transfer rates (more than 9M-Byte/s).

Access time	220ns
Data Storage (battery)	>2500h

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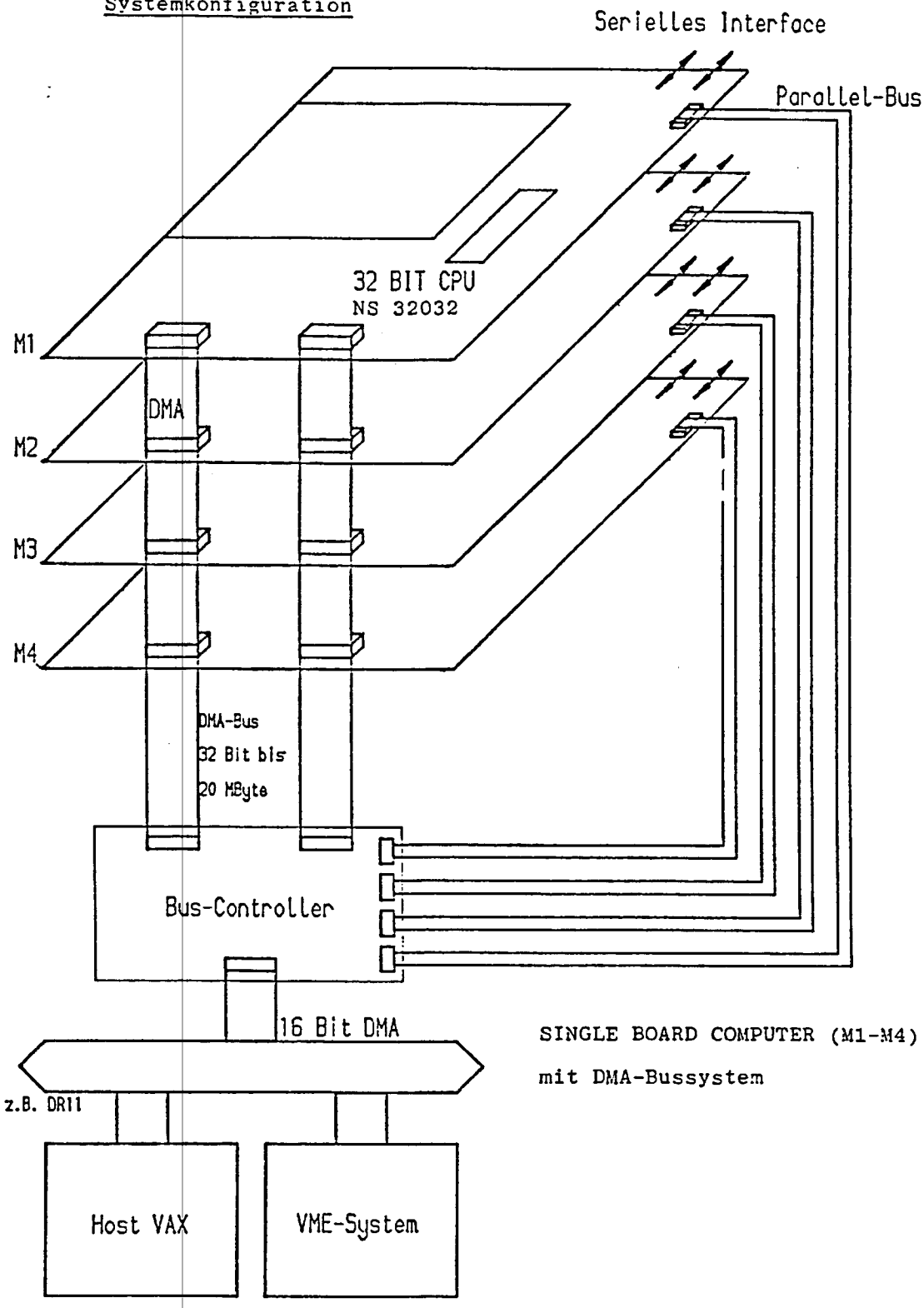
MAXI 32000 - SINGLE BOARD COMPUTER

Systemkonfiguration



SINGLE BOARD COMPUTER (M1-M4)

mit DMA-Bussystem

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