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The first 32bit "High Performance Single Board Computer" M A X I - 3 2 0 0 0

* 32bit CPU NS32032
* Virtuell memory management
* High speed floating point instructions
* up to 16Mbyte on board memory
* DMA channel with 20Mbytes/sec.
* Serial and parallel interfaces

The MAXI-32000 is an extremly high performance computer, one of the new generation. It was specially developed for use in field of data processing where unusual large amounts of data have to be processed at high speed.

Examples are:

Image processing
3D graphics
CAD/ CAM in general
Statistics
Numerical calculations
Quality control

Applications, where large memory banks are required and no mechanical parts are admissable.

Because of the high processing speed and the structure of the MAXI-32000, problems which up to now required equipment that would fill an indoor tennis court, air conditioned of course, can now be solved with one single board.

CPU

On the MAXI-32000 all circuits that belong to the NS32000 microprocessor family are represented.

These are in detail:

NS 32032 CPU Central Processing Unit
NS 32082 MMU Memory Managment Unit
NS 32201 TCU Timing Control Unit
NS 32081 FPU Floatint Point Unit
NS 32202 ICU Interrupt Control Unit

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With this configuration a parallel processor system whose capacity is comparable to that of a mainframe can be realised.

SERIAL CHANNELS

With the two on-board Zilog's-Z8530 there are four serial channels at the user's disposal, each of which have an enormous capability. They are used for communication with further computer terminals or peripheral equipment.

Apart from asychronous modes the user can realize complex protocolls such as HDLC/SDLC or BISYNC.
For higher transmission speed of up to 800kbaud two of the channels can be fitted out with differential line drivers (RS422).

PARALLEL I/O

For general purposes such as tape digitizer etc. a 20 bit parallel port is available. It can be used single bit wise in an input or output configuration. The in- and output buffers are HC or LS Schmitt-trigger and guarantee a maximum noise immunity.

INTERRUPT

All peripheral controllers, the SCC, the CIO and the DMA channel are interrupt controlled. In this way the CPU's spares any polling or supervisionary work.
In order to increase the flexibility of the system there are additionally 4 interrupt channels at one plug which can be used to solve current interface problems.

An on board timer is present in the system, able to generate interrupts with user-defined timing.

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This processor family enables us for the first time to work with micros in the same as way we would work with minis or mainframes.
All features which are accompanied with the "big ones" such as high data throughput, virtuell memory management, floating point instructions, two address structure, and many others have been realised with these chips. In spite of this high performance the still retain all the advantages of the micros:

easy to handle, low sensitivity with respect to climatic changes and an almost negligible power consumption.

Simply by using the FPU, numerical programms can be speeded up by a factor of nearly 100.

MEMORY

On the board there is an unsual large memory of 4Mbytes (basic version) or 16Mbytes (largest version). In this way one can load a complete 1000 x 1000 matrix including its inversion program.
With this high memory capacity the need of swapping programmes or data blocks becomes almost superfluous.
The memory, with byte parity, consists of 64k*1 or 256k*1 chips and can be addressed virtually by the MMU or directly linear.
In the case of a parity fault an NMI is generated to the CPU. The corresponding fault status can than be read from a status register.

DMA CHANNEL

The MAXI-32000 has no bus interface. In its place there is a high capacity DMA-channel. With these DMA interface data and programmes can be loaded or read to any points in the memory. The access can be carried out with bytes, words or double words. The maximum frequence therefore is 5Mhz which corresponds to 20Mbytes/s.
In this way the 16Mbyte memory can be completly loaded or read in approx. 850ms.
In order to transfer only the start address is externally loaded and all other addresses required are generated on the board itself.
For the main part the DMA channel was intended to be coupled with a host or an intelligent disk station.
It is however flexible enough to fullfill special demands based on timing and handshake signals without any significant alterations.

Additionally the DMA channel allows the coupeling of several (up to 16) MAXI-32000 !

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TECHNICAL DATA

MEMORY

The memory on the MAXI-32000 is general divided into two blocks. Each block is again into two banks. (Each bank consists of 4 data memories and 4 times 4 memories for the byte's parity bits).
When the processor is accessing actual the memory, the selected block receives the corresponding address for the access. A refresh cycle is carried out on the block that is not selected during the access.
If an access doesn't take place at least every 12 us it is then generated an automatic refresh every 15us covering the whole memory block.
If a memory access takes place during a refresh cycle, the access time is then extended to 420ns.
The speed of the memory system is sufficient to run with a 10MHz CPU without WAIT-STATES.
A Wait-State is automatically inserted if faster CPUs are being used.
The throughput of the processor is not dramatically effected by wait-states, this is because the processors in the NS32000 family have a pipeline, the advantage being that wait-states can be coped as they occur.
For special requirements the memory can be fitted with faster RAMs so that a 14MHz CPU work without wait-states.
The memory controller may generate an NMI to the CPU if a parity fault should occur during a read cycle.
When the NMI-routine is running the processor reads a register, which contains the parity status and can start further appropriate actions.

SERIAL INTERFACE

The MAXI-32000 is fitted with 4 serial interfaces.
2 of these interfaces can be very easily converted to RS422-interfaces by replacing the RS232 drivers with RS422 drivers.
Two Z8530-SCCs are used as controllers.
In this way, apart from asynchronous protocolls other sophisticated protocolls such as HDLC/SDLC or BISYNC can also be carried out without any further alterations.
All 4 channels have interrupt capabilities. Channels 1 and 2 have there interrupt vector themselves, the same applies to channel 3 and 4.

The following signals are at the users disposal on the serial side:

Transmitter

TxD	Transmitt Data
TxC	Transmitt Clock
DTR	Data Terminal Ready
RTS	Ready To Send

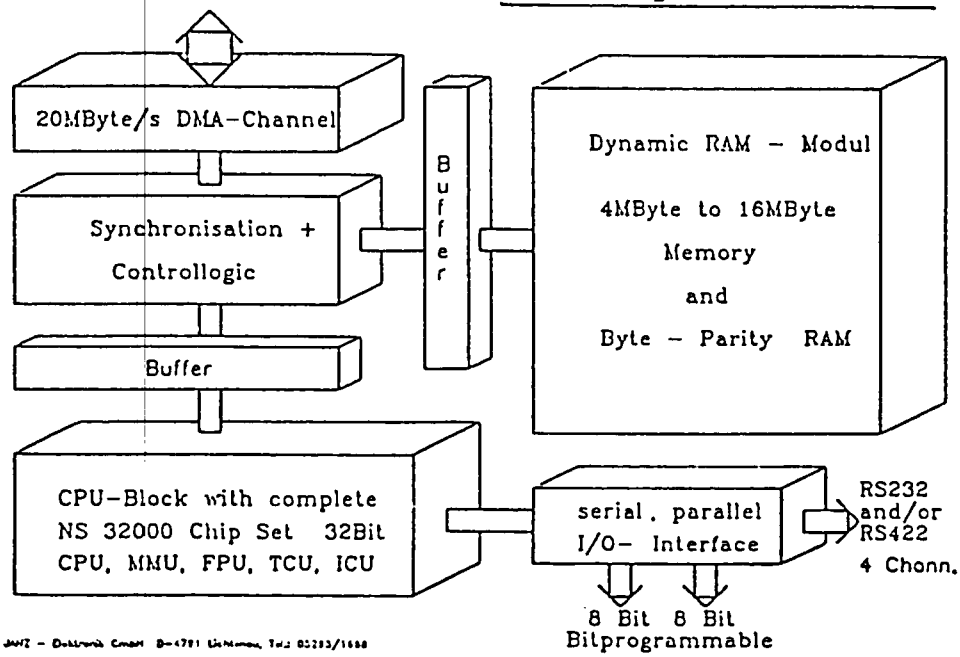
Receiver

RxD	Receive Data
RxC	Receive Clock
CTS	Clear To Send
DCD	Data Carrier Detect

PARALLEL CHANNELS

For general purposes the user has twenty bit free programmable I/Os at his disposal.
Every bits can be independently programmed as input or output.
The bits being programmed as inputs are in the position to generate interrupts by using definable external events.
For example H- or L levels, rising or falling edges.
The inputs can be logically combined to each other using an "and" or an "or". This allows interrupts to be generated on various bit patterns.
The inputs have a hysteresis of at least 0.8V, permitting a sufficient noise immunity.
With every 4 bits up to three counter/timers with internal or external clock can be programmed.
They also have apart from CKin and CKout further 2 control signals, TRIGGER and GATE.
4 additional in- and outputs are directly connected to the NS 32202 ICU. This simplifies the connection of the MAXI to a host, a diskstation or similar devices. If these interrupt possibilities should not be required they may then be used as 4 additional I/Os.

Blockdiagram MAXI32000



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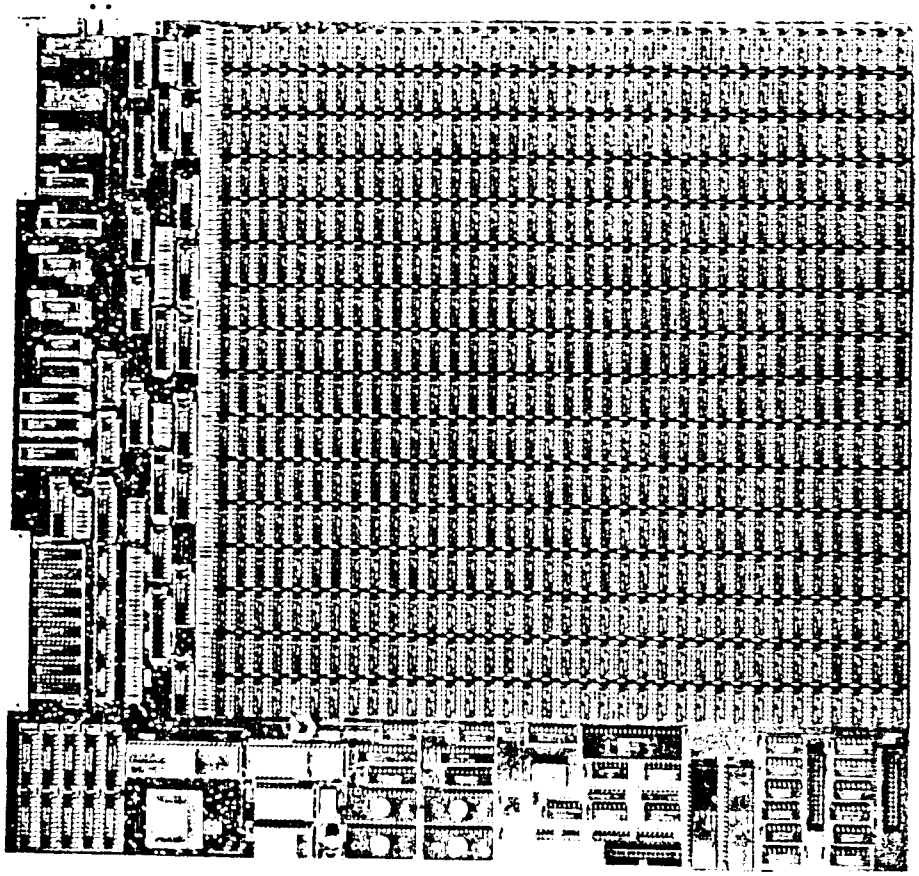
MAXI 32000



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